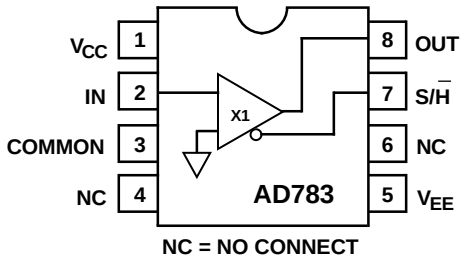
Complete Very High Speed Sample-and-Hold Amplifier

AD783*

FEATURES
Acquisition Time to 0.01%: 250 ns Typical
Low Power Dissipation: 95 mW
Low Droop Rate: 0.02 μV/μs
Fully Specified and Tested Hold Mode Distortion
Total Harmonic Distortion: –85 dB
Aperture Jitter: 50 ps Maximum
Internal Hold Capacitor
Self-Correcting Architecture
8-Pin Mini Cerdip and SOIC Packages

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD783 is a high speed, monolithic sample-and-hold amplifier (SHA). The AD783 offers a typical acquisition time of 250 ns to 0.01%. The AD783 is specified and tested for hold mode total harmonic distortion with input frequencies up to 100 kHz. The AD783 is configured as a unity gain amplifier and uses a patented self-correcting architecture that minimizes hold mode errors and ensures accuracy over temperature. The AD783 is self-contained and requires no external components or adjustments.

The AD783 retains the held value with a droop rate of 0.02 μV/μs. Excellent linearity and hold mode dc and dynamic performance make the AD783 ideal for high speed 12- and 14-bit analog-to-digital converters.

The AD783 is manufactured on Analog Devices' ABCMOS process which merges high performance, low noise bipolar circuitry with low power CMOS to provide an accurate, high speed, low power SHA.

The J grade device is specified for operation from 0°C to +70°C and the A grade from –40°C to +85°C. The J and A grades are available in 8-pin cerdip and SOIC packages. The military temperature range version is specified for operation from –55°C to +125°C and is available in an 8-pin cerdip package. For details refer to the *Analog Devices Military Products Databook* or AD783/883B data sheet.

***Protected by U.S. Patent Number 4,962,325.**

PRODUCT HIGHLIGHTS

1. Fast acquisition time (250 ns), low aperture jitter (20 ps) and fully specified hold mode distortion make the AD783 an ideal SHA for sampling systems.
2. Low droop (0.02 μV/μs) and internally compensated hold mode error result in superior system accuracy.
3. Low power (95 mW typical), complete functionality and small size make the AD783 an ideal choice for a variety of high performance applications.
4. The AD783 requires no external components or adjustments.
5. The AD783 is an excellent choice as a front-end SHA for high speed analog-to-digital converters such as the AD671, AD7586, AD674B, AD774B, AD7572 and AD7672.
6. Fully specified and tested hold mode distortion guarantees the performance of the SHA in sampled data systems.

REV. A

AD783–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{EE} = –5 V ± 5%, C_L = pF, unless otherwise noted)

Parameter	AD783J/A Min	Typ	Max	Units
SAMPLING CHARACTERISTICS				
Acquisition Time				
5 V Step to 0.01%		250	375	ns
5 V Step to 0.1%		200	350	ns
Small Signal Bandwidth		15		MHz
Full Power Bandwidth		2		MHz
HOLD CHARACTERISTICS				
Effective Aperture Delay (+25°C)	–30	15	30	ns
Aperture Jitter (+25°C)		20	50	ps
Hold Settling (to 1 mV, +25°C)		150	200	ns
Droop Rate		0.02	1	µV/µs
Feedthrough (+25°C)				
(V_{IN} = ±2.5 V, 500 kHz)		–80		dB
ACCURACY CHARACTERISTICS[1]				
Hold Mode Offset	–5	0	+5	mV
Hold Mode Offset Drift		10		µV/°C
Sample Mode Offset		50	200	mV
Nonlinearity		±0.005		% FS
Gain Error		±0.03	±0.1	% FS
OUTPUT CHARACTERISTICS				
Output Drive Current	–5		+5	mA
Output Resistance, DC		0.3	0.6	Ω
Total Output Noise (DC to 5 MHz)		150		µV rms
Sampled DC Uncertainty		85		µV rms
Hold Mode Noise (DC to 5 MHz)		125		µV rms
Short Circuit Current				
Source			20	mA
Sink			13	mA
INPUT CHARACTERISTICS				
Input Voltage Range	–2.5		+2.5	V
Bias Current		100	250	nA
Input Impedance		10		MΩ
Input Capacitance		2		pF
DIGITAL CHARACTERISTICS				
Input Voltage Low			0.8	V
Input Voltage High	2.0			V
Input Current High (V_{IN} = 5 V)		2	10	µA
POWER SUPPLY CHARACTERISTICS				
Operating Voltage Range	±4.75	±5	±5.25	V
Supply Current		9.5	17	mA
+PSRR (+5 V ± 5%)	45	65		dB
–PSRR (–5 V ± 5%)	45	65		dB
Power Consumption		95	175	mW
TEMPERATURE RANGE				
Specified Performance (J)	0		+70	°C
(A)	–40		+85	°C

NOTES

[1]Specified and tested over an input range of ±2.5 V.

Specifications subject to change without notice.

HOLD MODE AC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{EE} = –5 V ± 5%, C_L = 50 pF, unless otherwise noted)

Parameter	AD783J/A Min	Typ	Max	Units
TOTAL HARMONIC DISTORTION				
f_{IN} = 100 kHz		–85	–80	dB
f_{IN} = 500 kHz		–72		dB
SIGNAL-TO-NOISE AND DISTORTION				
f_{IN} = 100 kHz		77		dB
f_{IN} = 500 kHz		70		dB
INTERMODULATION DISTORTION				
(F1 = 99 kHz, F2 = 100 kHz)				
Second Order Products		–80		dB
Third Order Products		–85		dB

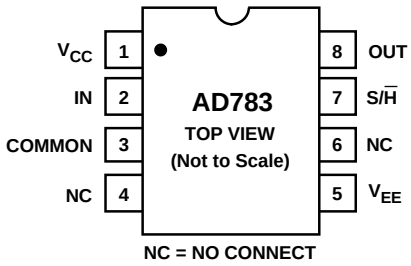
NOTES
[1]f_{IN} amplitude = 0 dB and f_{SAMPLE} = 300 kHz unless otherwise indicated.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Spec	With Respect to	Min	Max	Units
V_{CC}	COM	–0.5	+6.5	V
V_{EE}	COM	–6.5	+0.5	V
Analog Input	COM	–6.5	+6.5	V
Digital Input	COM	–0.5	+6.5	V
Output Short Circuit to Ground, V_{CC}, or V_{EE}		Indefinite		
Maximum Junction Temperature			+175	°C
Storage		–65	+150	°C
Lead Temperature (10 sec max)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD783 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model[1]	Temperature Range	Description	Package Options[2]
AD783JQ	0°C to +70°C	8-Pin Cerdip	Q-8
AD783AQ	–40°C to +85°C	8-Pin Cerdip	Q-8
AD783JR	0°C to +70°C	8-Pin SOIC	R-8
AD783AR	–40°C to +85°C	8-Pin SOIC	R-8

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD783/883B data sheet.
[2]Q = Cerdip, R = SOIC.

AD783 TO AD670 INTERFACE

The 15 MHz small signal bandwidth of the AD783 makes it a good choice for undersampling applications. Figure 8 shows the interface between the AD783 and the AD670 ADC, where the AD783 samples the incoming IF signal. For this particular application, the IF carrier was 10.7 MHz and the information signal was a 5 kHz FSK-modulated tone. The sample-and-hold signal is applied to the 8-bit AD670 ADC and then digitally processed for analysis.

The CLKIN signal is connected directly to the S/H pin of the AD783 and must comply with the acquisition and settling requirements of the SHA. A delayed version of CLKIN is applied to the R/$\overline{W}$ input of the AD670 in order to accommodate the hold-mode settling requirements of the AD783. The 10 µs conversion speed of the AD670 combined with the 150 ns hold-mode settling time of the AD783 result in a total system throughput of 10.15 µs.

By keeping the 10.7 MHz IF input to the AD783 at a low amplitude, 255 mV p-p, the resultant distortion and jitter-induced noise result in approximately 45 dB of dynamic range. The AD670 can be conveniently configured such that its full-scale input range is 255 mV in order to retain the full 8-bit dynamic range of the converter. The maximum sample rate of the AD670 is 10 µs; therefore, to comply with the Nyquist criteria the maximum information bandwidth is 50 kHz.

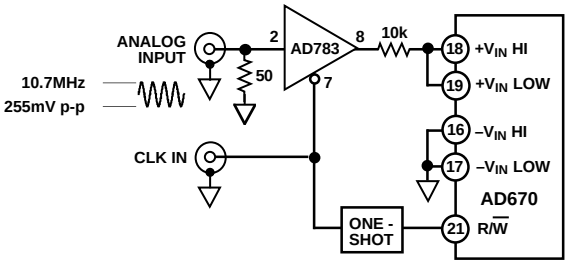


Figure 8. AD783 to AD670 Interface

AD783 to AD671 (12-Bit, 500 ns ADC) Interface

The AD783 to AD671 interface requires an op amp, a dual flip-flop, and a monostable multivibrator or "one-shot." The op amp amplifies the ±2.5 V output of the AD783 to the full-scale input of the AD671. Appropriate op amps include the AD841 and AD845 (see the AD671 data sheet for additional information). The flip-flops and one-shot are used to generate the AD671 ENCODE pulse and the appropriately timed AD783 S/H pulse.

A master sampling clock is tied to the clock input of flip-flop1 and the input of the one-shot. The D1 input of flip-flop1 should be tied high and the one-shot should be configured to generate a pulse on a rising edge of the sampling clock. The rising edge of the sampling clock causes the $\overline{Q1}$ output of the flip-flop to go low placing the AD783 into hold mode. Simultaneously, a low going pulse is generated at the one-shot output. The length of this pulse would usually be made long enough to allow the output of the AD783 to settle (hold-mode settling time), but because of the error-correcting ability of the AD671, the length of this pulse may be reduced to approximately 200 ns.

The low going one-shot output is connected to the clock input of flip-flop2. The D2 input of flip-flop2 is tied high. The rising edge of the low going pulse toggles the Q2 output of flip-flop2 to a high state. This output, which is tied to the ENCODE input of the AD671, initiates a conversion of the buffered output signal of the AD783. The AD671 issues the signal DAV when the conversion is complete. The DAV signal is tied to the asynchronous $\overline{CLR1}$ and $\overline{CLR2}$ inputs of both flip-flops. When DAV goes low, the $\overline{Q1}$ output goes high returning the AD783 to the sample or acquisition mode. The Q2 output (ENCODE) returns low until it is again triggered by the rising edge of the one-shot output.

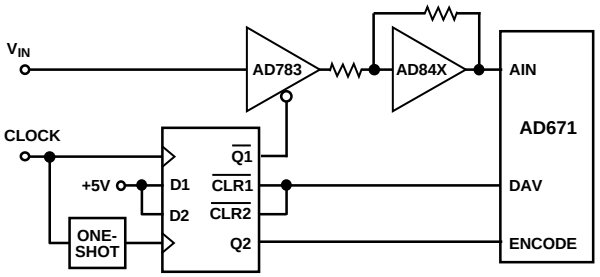
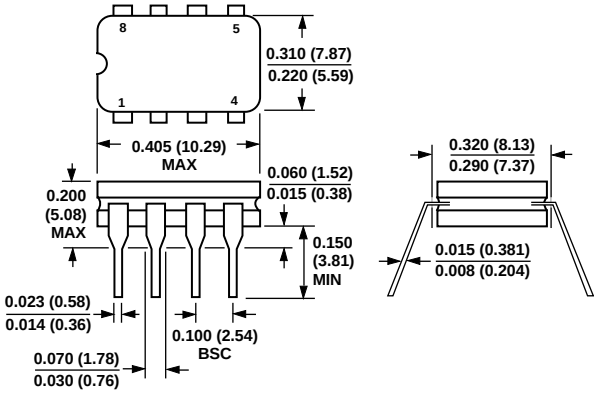


Figure 9. AD783 to AD671 Interface

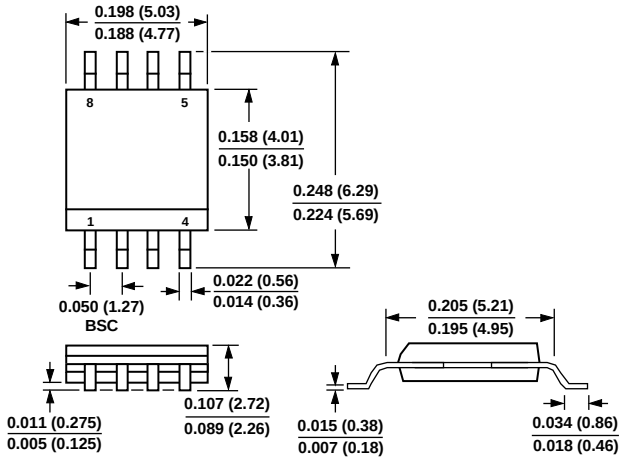
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Pin Cerdip (Q-8) Package



8-Pin SOIC (R-8) Package



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