

Product Overview

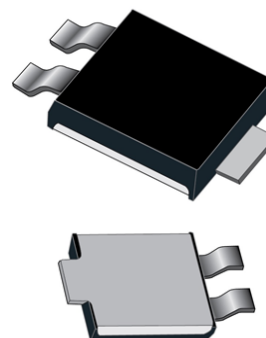
The Microchip UPS835L and UPS840e3 in Powermite 3 package, high efficiency rectifiers offer optimized forward voltage characteristics with reverse blocking capabilities of 35 and 40 volts. They are ideal for surface mount applications that operate at high frequencies. They offer high current/power capabilities previously only found in much larger packages.

In addition to its size advantages, Powermite 3 package features include a full metallic bottom that eliminates possibility of solder flux entrapment during assembly and a unique locking tab acts as an efficient heat path from die to mounting plane for external heat sinking with very low thermal resistance junction to case (bottom). Its innovative design makes this device ideal for use with automatic insertion equipment. RoHS compliant versions are available.

Features

- Low thermal resistance package for higher current operation
- Efficient heat path with integral locking bottom metal tab
- High current capability with low forward voltage
- Guard-ring die construction for transient protection
- Full metallic bottom eliminates flux entrapment
- Compatible with automatic insertion equipment
- Low profile-maximum height of 1.14 mm
- RoHS compliant versions available

Figure 1. Powermite 3 Package



Applications/Benefits

- Silicon Schottky (hot carrier) rectifier for minimal t_{rr} and minimal reverse recovery voltage
- Elimination of reverse-recovery oscillations to reduce need for EMI filtering
- For use in high-frequency switching power supplies, inverters, free-wheeling diode applications, charge pump circuits, and polarity protection applications
- Low forward power loss and high efficiency
- Low inductive parasitics (< 2 nH) for minimal $L (di/dt)$ effects
- Reduces reverse recovery loss with low I_{RM}
- Robust package configuration for pick-and-place handling
- Full-metallic bottom eliminates flux entrapment
- Small foot print (See [Pad Layout](#) details)

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1. Maximum Ratings

Table 1-1. Maximum Ratings at 25 °C Unless Otherwise Specified

Parameters/Test Conditions	Symbol	Value	Unit
Storage Temperature	T_{STG}	–55 to +150	°C
Junction Temperature	T_J	–55 to +125	°C
Working Peak Reverse Voltage	V_{RWM}	35	V
Peak Repetitive Reverse Voltage	V_{RRM}	40	V
DC Blocking Voltage	V_R	—	V
Thermal Resistance Junction-to-Ambient ¹	$R_{\theta JA}$	65	°C/W
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	3.0 2.5	°C/W
Average Rectified Output Current at $T_C = 75\text{ °C}$	I_O	8.0	A
Max Voltage Rate of Change	dV/dt	1,000	V/μs
Solder Temperature at 10 seconds	—	260	°C

Note:

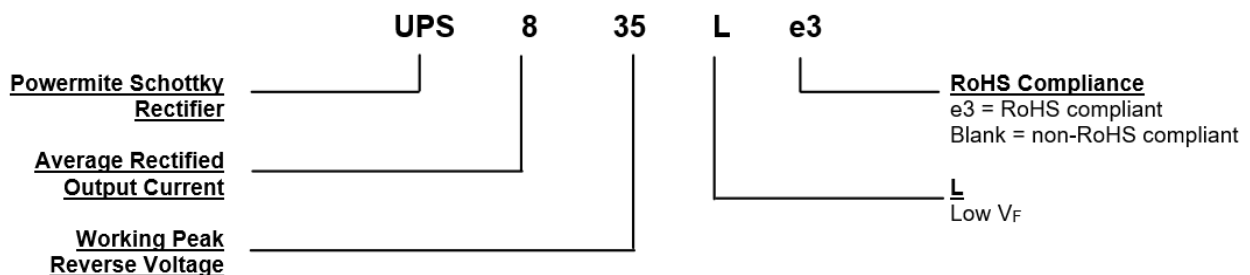
- On PCB with FR4 using 2 oz copper and recommended mounting pad size (see [Pad Layout](#))

1.1. Mechanical Packaging

- Case: Molded epoxy package meets UL94V-0
- Terminals: Copper with annealed matte-tin plating for RoHS compliance. Solderable per MIL-STD-750 method 2026.
(Consult factory for tin-lead plating).
- Marking: MSC, see electrical characteristics: device marking, date code
- Polarity: Cathode designated by heatsink/Tab 3. See [Schematic](#).
- Tape and Reel Option: Packaging per EIA-481-2 with 16 mm tape. Consult factory for quantities.
- Weight: Approximately 0.072 grams
- See [Package Dimensions](#)

1.2. Part Nomenclature

Figure 1-1. Part Nomenclature



2. Symbols and Definitions

Table 2-1. Symbols and Definitions

Symbol	Definition
C_T	Total Capacitance: The total small signal capacitance between the diode terminals of a complete device.
I_F	Forward Current: The dc current flowing from the external circuit into the anode terminal
I_{FSM}	Surge Peak Forward Current: The forward current including all nonrepetitive transient currents but excluding all repetitive transients (ref JESD282-B)
I_O	Average Rectified Output Current: The Output Current averaged over a full cycle with a 50 Hz or 60 Hz sine-wave input and a 180 degree conduction angle.
I_R	Reverse Current: The dc current flowing from the external circuit into the cathode terminal at the specified voltage V_R
$V_{(BR)}$	Breakdown Voltage: A voltage in the breakdown region.
V_F	Forward Voltage: A positive dc anode-cathode voltage the device will exhibit at a specified forward current.
V_R	Reverse Voltage: A positive dc cathode-anode voltage below the breakdown region
$V_{R(RMS)}$	Reverse Voltage: Root-Mean-Square value of alternating component of a positive dc cathode-anode voltage
V_{RRM}	Repetitive Peak Reverse Voltage: The peak reverse voltage including all repetitive transient voltages but excluding all non-repetitive transient voltages.
V_{RWM}	Working Peak Reverse Voltage: The peak voltage excluding all transient voltages (ref JESD282-B). Also sometimes known historically as PIV.

2.1. Electrical Characteristics

Table 2-2. Electrical Characteristics

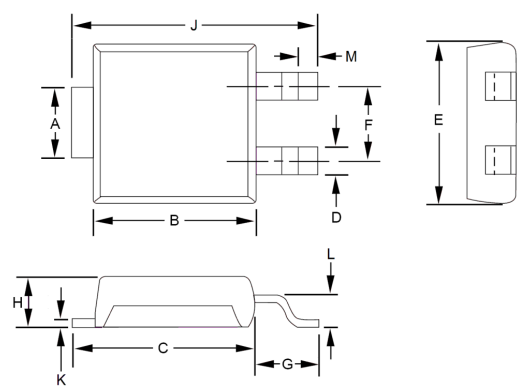
Part Number	Device Marking ¹	Working Peak Reverse Voltage	Max Reverse Current ²	RMS Reverse Voltage	Max Reverse Breakdown Voltage ²		Max Forward Voltage ² V_F				Max Forward Surge Current	Capacitance at $V_R = 4V$ at $f = 1 MHz$	Maximum Voltage Rate of Change
		V_{RWM}	I_R at V_{RWM}	$V_{R(RMS)}$	V_{BR} at I_{BR}	I_{BR}	at 3A	at 8A	at 10A	at 15A	I_{FSM}	C_T	dV/dt
		V	mA	V	V	mA	V	V	V	V	A	pF	V/ μs
UPS835L	S835	35	1.4	24.5	35	1.4	—	0.51	—	—	100	—	1,000
UPS840	S840	40	0.5	28	40	0.5	0.39	0.45	0.49	0.535	150	700	1,000

Notes:

1. Include • in marking for e3 parts (e.g. UPS760e3 and S760•)
2. Short duration test pulse used to minimize self-heating effect

3. Package Dimensions

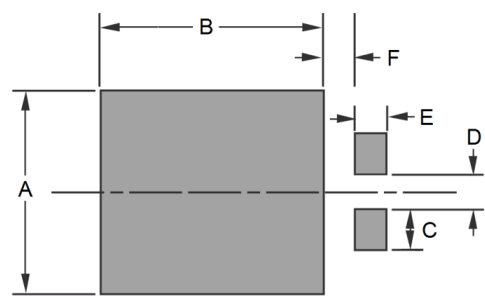
Figure 3-1. Package Dimensions



Dim.	Inch		Millimeters	
	Min.	Max.	Min.	Max.
A	0.068	0.072	1.73	1.83
B	0.172	0.174	4.37	4.43
C	0.197	0.204	5.01	5.17
D	0.035 NOM		0.889 NOM	
E	0.159	0.161	4.03	4.09
F	0.072 NOM		1.83 NOM	
G	0.056 NOM		1.422 NOM	
H	0.043	0.045	1.10	1.14
J	0.252	0.260	6.40	6.61
K	0.007 NOM		0.178 NOM	
L	0.028	0.030	0.71	0.77
M	0.014	0.018	0.36	0.46

3.1. Pad Layout

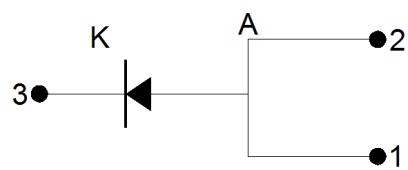
Figure 3-2. Pad Layout



Dim.	Inch	Millimeters
	Nominal	Nominal
A	0.190	4.826
B	0.210	5.344
C	0.038	0.965
D	0.034	0.864
E	0.030	0.762
F	0.030	0.762

3.2. Schematic

Figure 3-3. Schematic



4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	04/2025	Document was converted to Microchip template and assigned literature number DS00005924.
Rev. D	04/2024	Microsemi document was created and assigned literature number RF01102.

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