

# 5 V ECL Coaxial Cable Driver

## MC10EL89

### Description

The MC10EL89 is a differential fanout gate specifically designed to drive coaxial cables. The device is especially useful in Digital Video Broadcasting applications; for this application, since the system is polarity free, each output can be used as an independent driver. The driver boasts a gain of approximately 40 and produces output swings twice as large as a standard ECL output. When driving a coaxial cable, proper termination is required at both ends of the line to minimize signal loss. The 1.6 V output swings allow for termination at both ends of the cable, while maintaining the required 800 mV swing at the receiving end of the cable. Because of the larger output swings, the device cannot be terminated into the standard -2.0 V. All of the DC parameters are tested with a 50  $\Omega$  to -3.0 V load. The driver accepts a standard differential ECL input and can run off of the Digital Video Broadcast standard -5.0 V supply.

### Features

- 375 ps Propagation Delay
- 1.6 V Output Swings
- PECL Mode Operating Range:
  - ♦  $V_{CC} = 4.2 \text{ V to } 5.7 \text{ V}$  with  $V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:
  - ♦  $V_{CC} = 0 \text{ V}$  with  $V_{EE} = -4.2 \text{ V to } -5.7 \text{ V}$
- Internal Input Pulldown Resistors
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

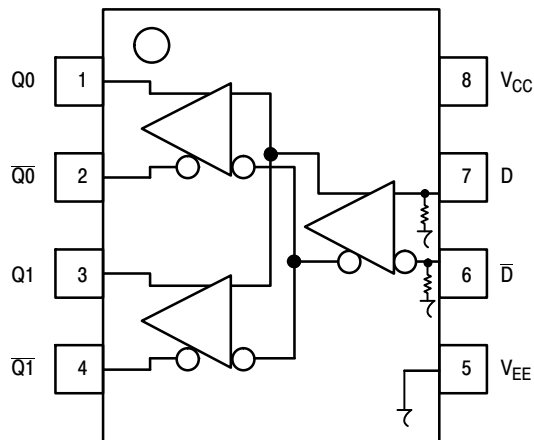
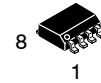
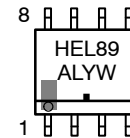


Figure 1. Logic Diagram and Pinout Assignment



SOIC-8 NB  
 D SUFFIX  
 CASE 751-07

### MARKING DIAGRAM



A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 M = Date Code  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

| Device       | Package          | Shipping†        |
|--------------|------------------|------------------|
| MC10EL89DG   | SOIC-8 (Pb-Free) | 98 Units/Tube    |
| MC10EL89DR2G | SOIC-8 (Pb-Free) | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# MC10EL89

**Table 1. PIN DESCRIPTION**

| PIN                             | Function                                |
|---------------------------------|-----------------------------------------|
| D, $\bar{D}$                    | ECL Data Inputs                         |
| Q0, $\bar{Q0}$ ; Q1, $\bar{Q1}$ | ECL Data Outputs (1.6 V <sub>pp</sub> ) |
| V <sub>CC</sub>                 | Positive Supply                         |
| V <sub>EE</sub>                 | Negative Supply                         |

**Table 2. ATTRIBUTES**

| Characteristics                                               | Value                |
|---------------------------------------------------------------|----------------------|
| Internal Input Pulldown Resistor                              | 50 K $\Omega$        |
| Internal Input Pullup Resistor                                | N/A                  |
| ESD Protection<br>Human Body Model<br>Machine Model           | > 2 kV<br>> 100 V    |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Level 1              |
| Flammability Rating<br>Oxygen Index: 28 to 34                 | UL 94 V-0 @ 0.125 in |
| Transistor Count                                              | 31                   |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test        |                      |

1. For additional information, see Application Note [AND8003/D](#).

**Table 3. MAXIMUM RATINGS**

| Symbol           | Parameter                                          | Condition 1                                    | Condition 2                                                                    | Rating      | Unit |
|------------------|----------------------------------------------------|------------------------------------------------|--------------------------------------------------------------------------------|-------------|------|
| V <sub>CC</sub>  | PECL Mode Power Supply                             | V <sub>EE</sub> = 0 V                          |                                                                                | 8           | V    |
| V <sub>EE</sub>  | NECL Mode Power Supply                             | V <sub>CC</sub> = 0 V                          |                                                                                | -8          | V    |
| V <sub>I</sub>   | PECL Mode Input Voltage<br>NECL Mode Input Voltage | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> $\leq$ V <sub>CC</sub><br>V <sub>I</sub> $\geq$ V <sub>EE</sub> | 6<br>-6     | V    |
| I <sub>out</sub> | Output Current                                     | Continuous<br>Surge                            |                                                                                | 50<br>100   | mA   |
| T <sub>A</sub>   | Operating Temperature Range                        |                                                |                                                                                | -40 to +85  | °C   |
| T <sub>stg</sub> | Storage Temperature Range                          |                                                |                                                                                | -65 to +150 | °C   |
| $\theta_{JA}$    | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | SOIC-8                                                                         | 190<br>130  | °C/W |
| $\theta_{JC}$    | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | SOIC-8                                                                         | 41 to 44    | °C/W |
| T <sub>sol</sub> | Wave Solder (Pb-Free)                              | <2 to 3 sec @ 260°C                            |                                                                                | 265         | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

# MC10EL89

**Table 4. 10EL SERIES PECL DC CHARACTERISTICS** ( $V_{CC} = 5.0 \text{ V}$ ;  $V_{EE} = 0.0 \text{ V}$  (Note 1))

| Symbol      | Characteristic                                                             | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|----------------------------------------------------------------------------|-------|------|------|------|------|------|------|------|------|---------------|
|             |                                                                            | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current                                                       |       | 23   | 28   |      | 23   | 28   |      | 23   | 28   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 2)                                               | 3.77  | 3.90 | 4.02 | 3.87 | 3.98 | 4.10 | 3.94 | 4.04 | 4.19 | V             |
| $V_{OL}$    | Output LOW Voltage (Note 2)                                                | 2.10  | 2.28 | 2.42 | 2.00 | 2.30 | 2.44 | 1.95 | 2.33 | 2.49 | V             |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                          | 3770  |      | 4110 | 3870 |      | 4190 | 3940 |      | 4280 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                           | 3050  |      | 3500 | 3050 |      | 3520 | 3050 |      | 3555 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.5   |      | 4.6  | 2.5  |      | 4.6  | 2.5  |      | 4.6  | V             |
| $I_{IH}$    | Input HIGH Current                                                         |       | 70   | 150  |      | 50   | 150  |      | 40   | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                                          | 0.5   | 50   |      | 0.5  | 30   |      | 0.3  | 25   |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $+0.25 \text{ V} / -0.5 \text{ V}$ .
2. Outputs are terminated through a  $50 \Omega$  resistor to  $V_{CC} - 3.0 \text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1 \text{ V}$ .

**Table 5. 10EL SERIES NECL DC CHARACTERISTICS** ( $V_{CC} = 0.0 \text{ V}$ ;  $V_{EE} = -5.0 \text{ V}$  (Note 1))

| Symbol      | Characteristic                                                             | -40°C |       |       | 25°C  |       |       | 85°C  |       |       | Unit          |
|-------------|----------------------------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
|             |                                                                            | Min   | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current                                                       |       | 23    | 28    |       | 23    | 28    |       | 23    | 28    | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 2)                                               | -1.23 | -1.10 | -0.98 | -1.13 | -1.02 | -0.90 | -1.06 | -0.96 | -0.81 | V             |
| $V_{OL}$    | Output LOW Voltage (Note 2)                                                | -2.90 | -2.72 | -2.58 | -3.00 | -2.70 | -2.56 | -3.05 | -2.67 | -2.51 | V             |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                          | -1230 |       | -890  | -1130 |       | -810  | -1060 |       | -720  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                           | -1950 |       | -1500 | -1950 |       | -1480 | -1950 |       | -1445 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | -2.5  |       | -0.4  | -2.5  |       | -0.4  | -2.5  |       | -0.4  | V             |
| $I_{IH}$    | Input HIGH Current                                                         |       | 70    | 150   |       | 50    | 150   |       | 20    | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                                          | 0.5   | 50    |       | 0.5   | 30    |       | 0.3   | 25    |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

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2. Outputs are terminated through a  $50 \Omega$  resistor to  $V_{CC} - 3.0 \text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1 \text{ V}$ .

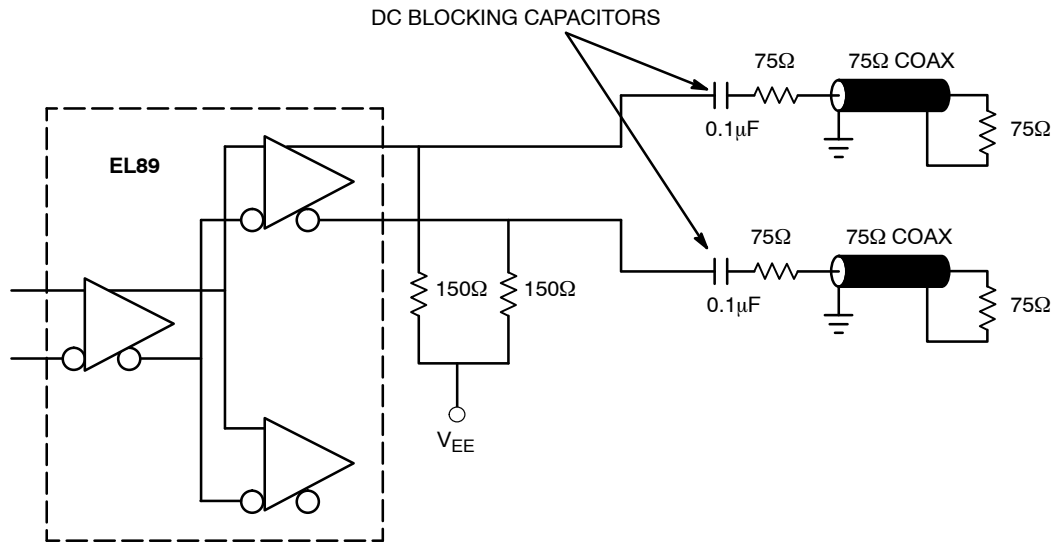
# MC10EL89

**Table 6. AC CHARACTERISTICS** ( $V_{CC} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 1))

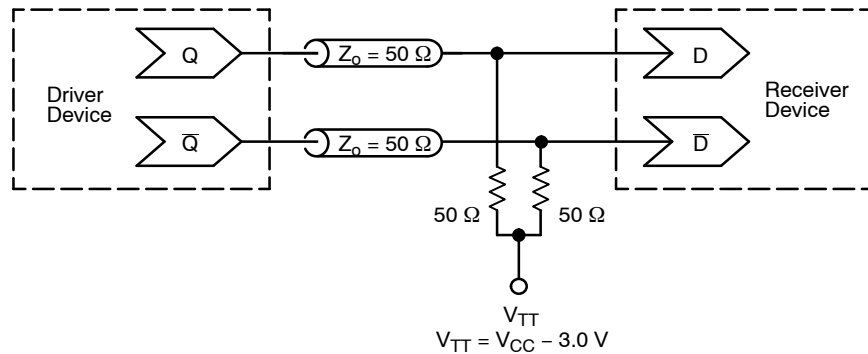
| Symbol                 | Characteristic                          | -40°C |     |     | 25°C |     |     | 85°C |     |     | Unit |
|------------------------|-----------------------------------------|-------|-----|-----|------|-----|-----|------|-----|-----|------|
|                        |                                         | Min   | Typ | Max | Min  | Typ | Max | Min  | Typ | Max |      |
| $f_{\max}$             | Maximum Toggle Frequency                |       |     |     |      | 1.5 |     |      |     |     | Gb/s |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay to Output             | 200   | 340 | 480 | 260  | 350 | 440 | 310  | 400 | 490 | ps   |
| $t_{SKEW}$             | Within-Device Skew                      |       | 5   | 20  |      | 5   | 20  |      | 5   | 20  | ps   |
| $t_{JITTER}$           | Random Clock Jitter (RMS)               |       | 5   |     |      | 5   |     |      | 5   |     | ps   |
| $V_{PP}$               | Input Swing (Note 2)                    | 150   |     |     | 150  | 400 |     | 150  |     |     | mV   |
| $t_r$<br>$t_f$         | Output Rise/Fall Times Q<br>(20% – 80%) | 205   | 330 | 455 | 205  | 330 | 455 | 205  | 330 | 455 | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- $V_{EE}$  can vary  $+0.25\text{ V}$  /  $-0.5\text{ V}$ .
- $V_{PP(\min)}$  is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of  $\approx 40$ .



**Figure 2. EL89 CATV Termination Configuration**



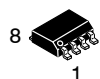
**Figure 3. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

## MC10EL89

### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

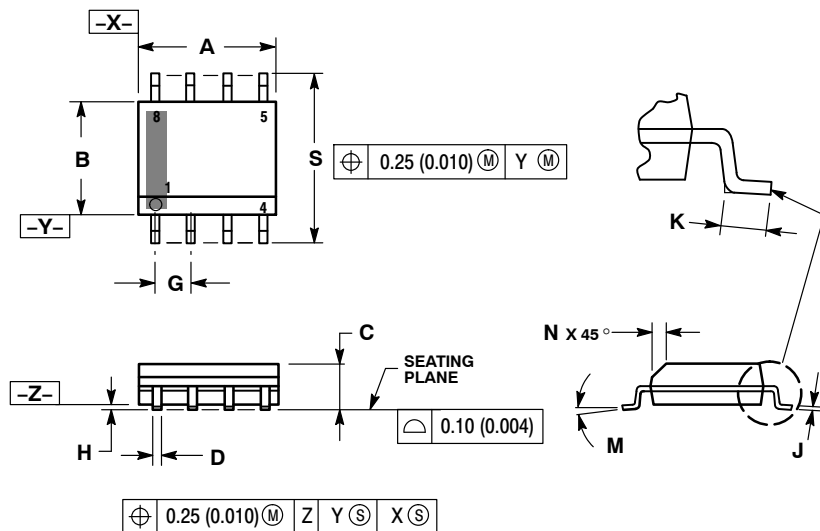
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SCALE 1:1

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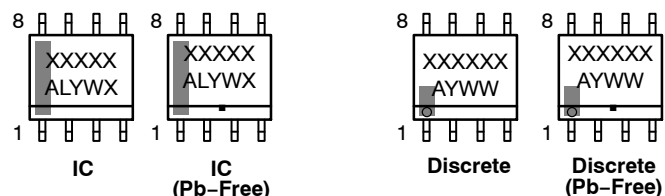
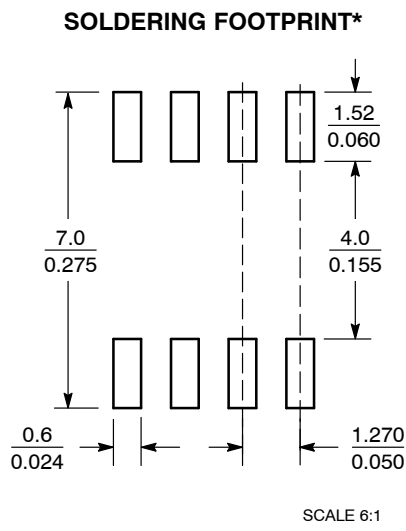


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

GENERIC  
MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
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\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

|                  |             |                                                                                                                                                                                  |
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|                                                                                                                                                                                                   |                                                                                                                                                                                          |                                                                                                                                                                                    |                                                                                                                                                                                                        |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>STYLE 1:</b><br>PIN 1. EMITTER<br>2. COLLECTOR<br>3. COLLECTOR<br>4. EMITTER<br>5. EMITTER<br>6. BASE<br>7. BASE<br>8. EMITTER                                                                 | <b>STYLE 2:</b><br>PIN 1. COLLECTOR, DIE, #1<br>2. COLLECTOR, #1<br>3. COLLECTOR, #2<br>4. COLLECTOR, #2<br>5. BASE, #2<br>6. EMITTER, #2<br>7. BASE, #1<br>8. EMITTER, #1               | <b>STYLE 3:</b><br>PIN 1. DRAIN, DIE #1<br>2. DRAIN, #1<br>3. DRAIN, #2<br>4. DRAIN, #2<br>5. GATE, #2<br>6. SOURCE, #2<br>7. GATE, #1<br>8. SOURCE, #1                            | <b>STYLE 4:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE<br>4. ANODE<br>5. ANODE<br>6. ANODE<br>7. ANODE<br>8. COMMON CATHODE                                                                           |
| <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. DRAIN<br>3. DRAIN<br>4. DRAIN<br>5. GATE<br>6. GATE<br>7. SOURCE<br>8. SOURCE                                                                               | <b>STYLE 6:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. DRAIN<br>4. SOURCE<br>5. SOURCE<br>6. GATE<br>7. GATE<br>8. SOURCE                                                                    | <b>STYLE 7:</b><br>PIN 1. INPUT<br>2. EXTERNAL BYPASS<br>3. THIRD STAGE SOURCE<br>4. GROUND<br>5. DRAIN<br>6. GATE 3<br>7. SECOND STAGE Vd<br>8. FIRST STAGE Vd                    | <b>STYLE 8:</b><br>PIN 1. COLLECTOR, DIE #1<br>2. BASE, #1<br>3. BASE, #2<br>4. COLLECTOR, #2<br>5. COLLECTOR, #2<br>6. EMITTER, #2<br>7. EMITTER, #1<br>8. COLLECTOR, #1                              |
| <b>STYLE 9:</b><br>PIN 1. EMITTER, COMMON<br>2. COLLECTOR, DIE #1<br>3. COLLECTOR, DIE #2<br>4. EMITTER, COMMON<br>5. EMITTER, COMMON<br>6. BASE, DIE #2<br>7. BASE, DIE #1<br>8. EMITTER, COMMON | <b>STYLE 10:</b><br>PIN 1. GROUND<br>2. BIAS 1<br>3. OUTPUT<br>4. GROUND<br>5. GROUND<br>6. BIAS 2<br>7. INPUT<br>8. GROUND                                                              | <b>STYLE 11:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. DRAIN 2<br>7. DRAIN 1<br>8. DRAIN 1                                               | <b>STYLE 12:</b><br>PIN 1. SOURCE<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                                 |
| <b>STYLE 13:</b><br>PIN 1. N.C.<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                              | <b>STYLE 14:</b><br>PIN 1. N-SOURCE<br>2. N-GATE<br>3. P-SOURCE<br>4. P-GATE<br>5. P-DRAIN<br>6. P-DRAIN<br>7. N-DRAIN<br>8. N-DRAIN                                                     | <b>STYLE 15:</b><br>PIN 1. ANODE 1<br>2. ANODE 1<br>3. ANODE 1<br>4. ANODE 1<br>5. CATHODE, COMMON<br>6. CATHODE, COMMON<br>7. CATHODE, COMMON<br>8. CATHODE, COMMON               | <b>STYLE 16:</b><br>PIN 1. EMITTER, DIE #1<br>2. BASE, DIE #1<br>3. EMITTER, DIE #2<br>4. BASE, DIE #2<br>5. COLLECTOR, DIE #2<br>6. COLLECTOR, DIE #2<br>7. COLLECTOR, DIE #1<br>8. COLLECTOR, DIE #1 |
| <b>STYLE 17:</b><br>PIN 1. VCC<br>2. V2OUT<br>3. V1OUT<br>4. TXE<br>5. RXE<br>6. VEE<br>7. GND<br>8. ACC                                                                                          | <b>STYLE 18:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. CATHODE<br>8. CATHODE                                                                 | <b>STYLE 19:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. MIRROR 2<br>7. DRAIN 1<br>8. MIRROR 1                                             | <b>STYLE 20:</b><br>PIN 1. SOURCE (N)<br>2. GATE (N)<br>3. SOURCE (P)<br>4. GATE (P)<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                   |
| <b>STYLE 21:</b><br>PIN 1. CATHODE 1<br>2. CATHODE 2<br>3. CATHODE 3<br>4. CATHODE 4<br>5. CATHODE 5<br>6. COMMON ANODE<br>7. COMMON ANODE<br>8. CATHODE 6                                        | <b>STYLE 22:</b><br>PIN 1. I/O LINE 1<br>2. COMMON CATHODE/VCC<br>3. COMMON CATHODE/VCC<br>4. I/O LINE 3<br>5. COMMON ANODE/GND<br>6. I/O LINE 4<br>7. I/O LINE 5<br>8. COMMON ANODE/GND | <b>STYLE 23:</b><br>PIN 1. LINE 1 IN<br>2. COMMON ANODE/GND<br>3. COMMON ANODE/GND<br>4. LINE 2 IN<br>5. LINE 2 OUT<br>6. COMMON ANODE/GND<br>7. COMMON ANODE/GND<br>8. LINE 1 OUT | <b>STYLE 24:</b><br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR/ANODE<br>4. COLLECTOR/ANODE<br>5. CATHODE<br>6. CATHODE<br>7. COLLECTOR/ANODE<br>8. COLLECTOR/ANODE                                      |
| <b>STYLE 25:</b><br>PIN 1. VIN<br>2. N/C<br>3. REXT<br>4. GND<br>5. IOUT<br>6. IOUT<br>7. IOUT<br>8. IOUT                                                                                         | <b>STYLE 26:</b><br>PIN 1. GND<br>2. dv/dt<br>3. ENABLE<br>4. ILIMIT<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. VCC                                                                    | <b>STYLE 27:</b><br>PIN 1. ILIMIT<br>2. OVLO<br>3. UVLO<br>4. INPUT+<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. DRAIN                                                            | <b>STYLE 28:</b><br>PIN 1. SW_TO_GND<br>2. DASIC_OFF<br>3. DASIC_SW_DET<br>4. GND<br>5. V_MON<br>6. VBULK<br>7. VBULK<br>8. VIN                                                                        |
| <b>STYLE 29:</b><br>PIN 1. BASE, DIE #1<br>2. EMITTER, #1<br>3. BASE, #2<br>4. EMITTER, #2<br>5. COLLECTOR, #2<br>6. COLLECTOR, #2<br>7. COLLECTOR, #1<br>8. COLLECTOR, #1                        | <b>STYLE 30:</b><br>PIN 1. DRAIN 1<br>2. DRAIN 1<br>3. GATE 2<br>4. SOURCE 2<br>5. SOURCE 1/DRAIN 2<br>6. SOURCE 1/DRAIN 2<br>7. SOURCE 1/DRAIN 2<br>8. GATE 1                           |                                                                                                                                                                                    |                                                                                                                                                                                                        |

|                         |                    |                                                                                                                                                                                     |
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