HARRIS Semiconductor

RFD15P05, RFD15P05SM, RFP15P05

-15A, -50V, 0.150 Ohm, P-Channel Power MOSFETs

September 1998

Features

- **-15A, -50V**
- **$r_{DS(ON)}$ = 0.150Ω**
- ***Temperature Compensating* PSPICE Model**
- **Peak Current vs Pulse Width Curve**
- **UIS Rating Curve**
- **Related Literature**
  - **TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"**

Description

These are P-Channel power MOSFETs manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

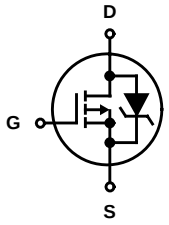
Formerly developmental type TA09833.

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFD15P05	TO-251AA	D15P05
RFD15P05SM	TO-252AA	D15P05
RFP15P05	TO-220AB	RFP15P05

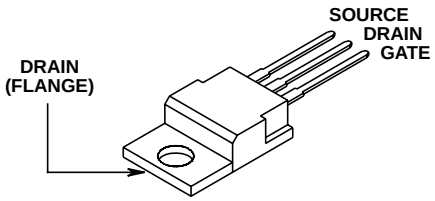
NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD15P05SM9A.

Symbol

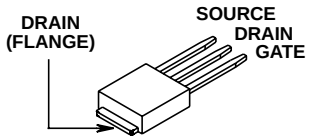


Packaging

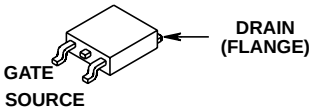
JEDEC TO-220AB



JEDEC TO-251AA



JEDEC TO-252AA



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2387.4**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFD15P05, RFD15P05SM, RFP15P05	UNITS
Drain Source Voltage (Note 1)	V_{DSS}	-50	V
Drain Gate Voltage (R_G = 20KΩ) (Note 1)	V_{DGR}	-50	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current Continuous	I_D	-15	A
Pulsed (Note 3)	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation	P_D	80	W
Derate above 25^oC		0.533	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 11)		-50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA		-2.0	-	-4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}		-	-	-1	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, $T_C = 150^oC$		-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 15A, V_{GS} = -10V (Figure 9)		-	-	0.150	Ω
Turn-On Time	t_{ON}	V_{DD} = -25V, $I_D \approx$ 7.5A, R_G = 12.5Ω, R_L = 3.3Ω, V_{GS} = -10V (Figures 16, 17)		-	-	60	ns
Turn-On Delay Time	$t_{D(ON)}$			-	16	-	ns
Rise Time	t_R			-	30	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	50	-	ns
Fall Time	t_F			-	20	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0V to -20V	V_{DD} = -40V, I_D = 15A, R_L = 2.67Ω, $I_{G(REF)}$ = -0.65mA (Figures 18, 19)	-	-	150	nC
Gate Charge at -10V	$Q_{G(-10)}$	V_{GS} = 0V to -10V		-	-	75	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0V to -2V		-	-	3.5	nC
Input Capacitance	C_{ISS}	V_{DS} = -25V, V_{GS} = 0V f = 1MHz (Figure 12)		-	1150	-	pF
Output Capacitance	C_{OSS}			-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	56	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-220AB, TO-251AA, TO-252AA		-	-	1.875	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251AA, TO-252AA		-	-	100	$^oC/W$
		TO-220AB		-	-	62.5	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = -15A	-	-	-1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = -15A, dI_{SD}/dt = -100A/μs	-	-	125	ns

NOTES:

2. Pulse test: pulse duration ≤ 300ms, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).

Typical Performance Curves

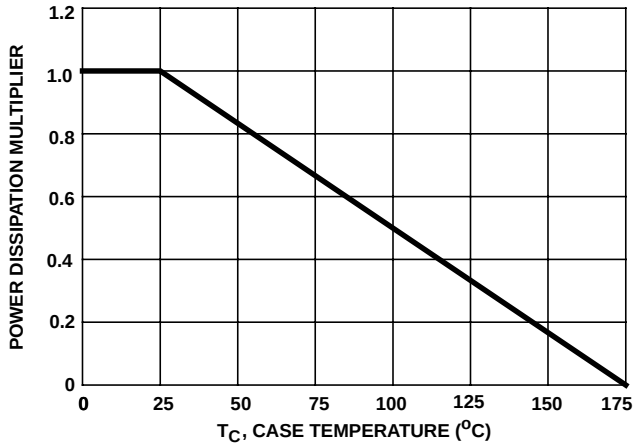


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

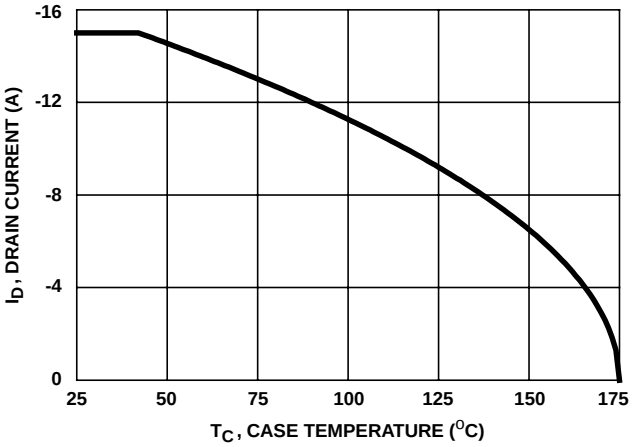


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

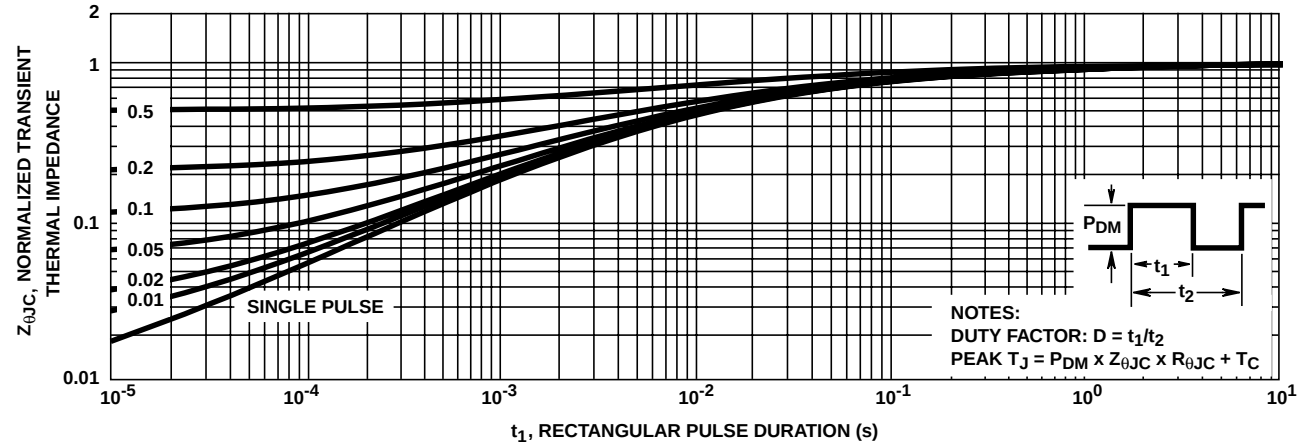


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

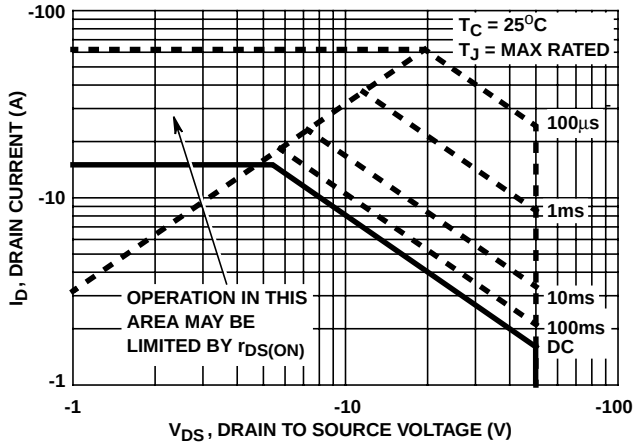


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

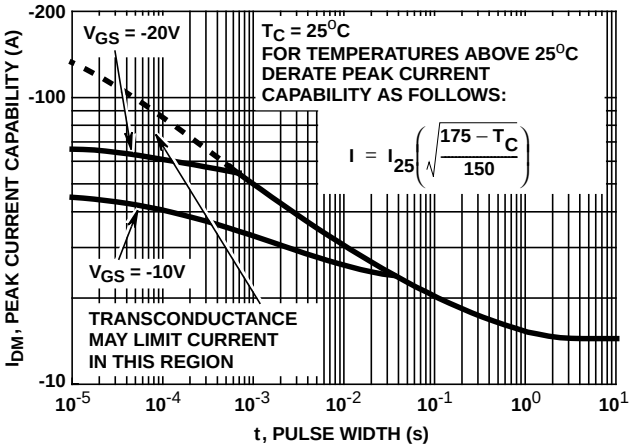


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

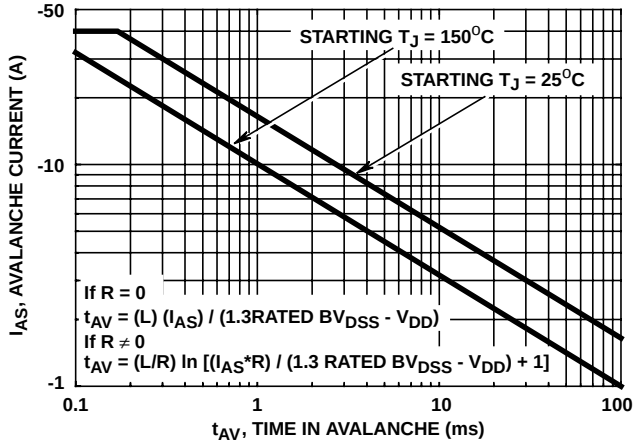


FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

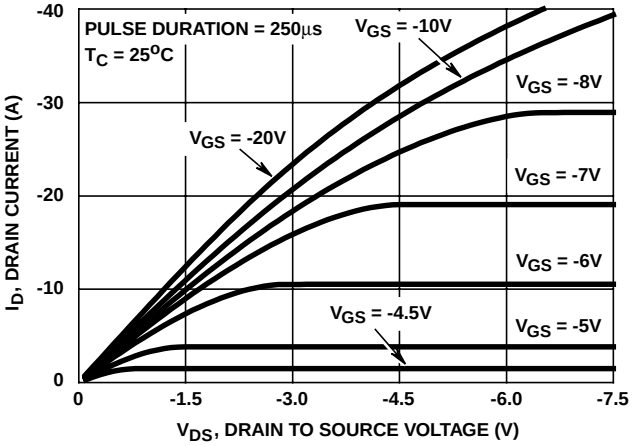


FIGURE 7. SATURATION CHARACTERISTICS

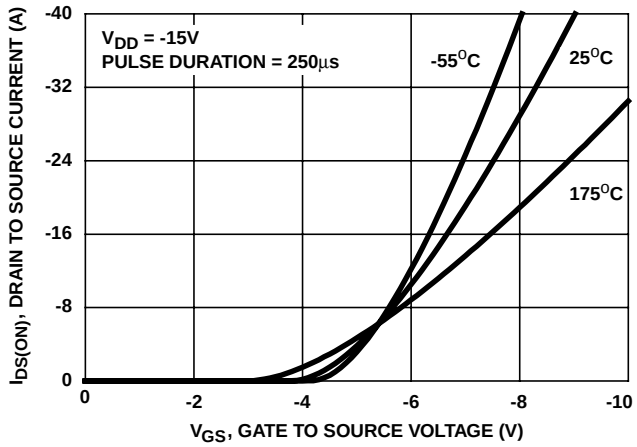


FIGURE 8. TRANSFER CHARACTERISTICS

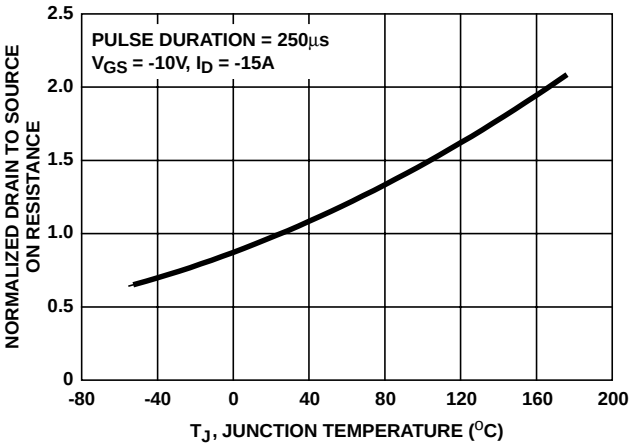


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

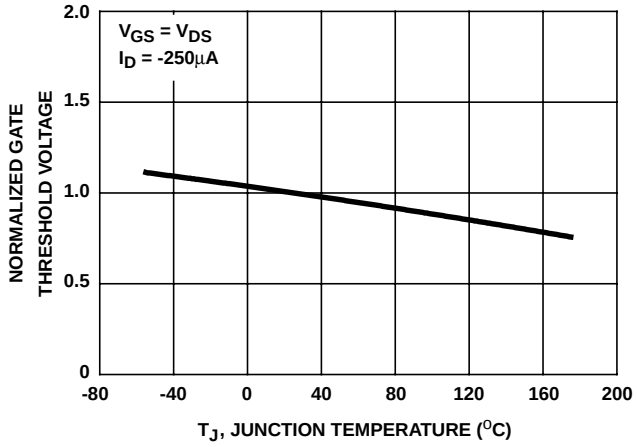


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

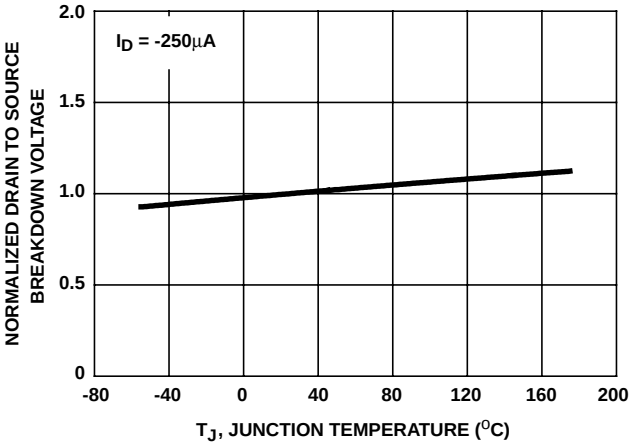


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

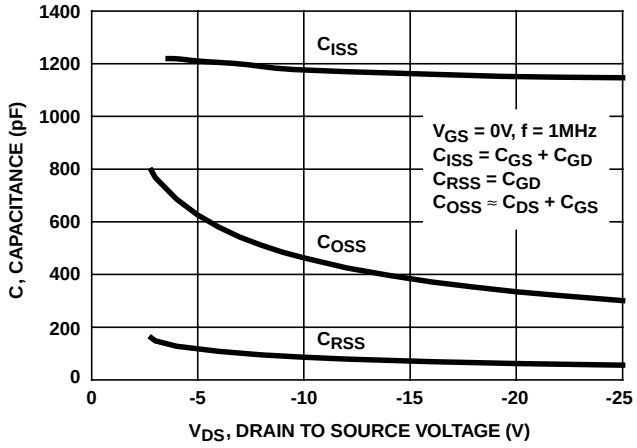
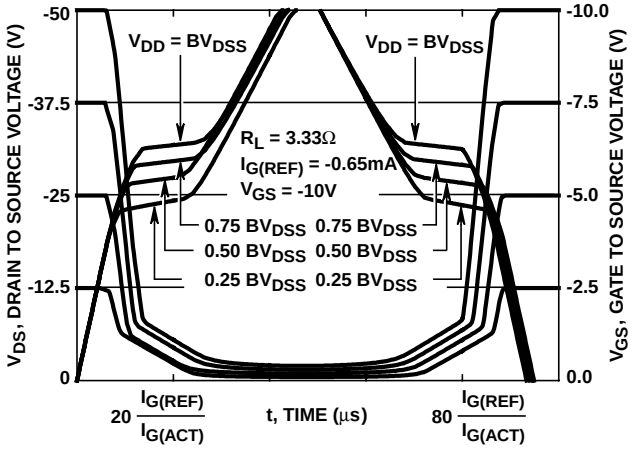


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

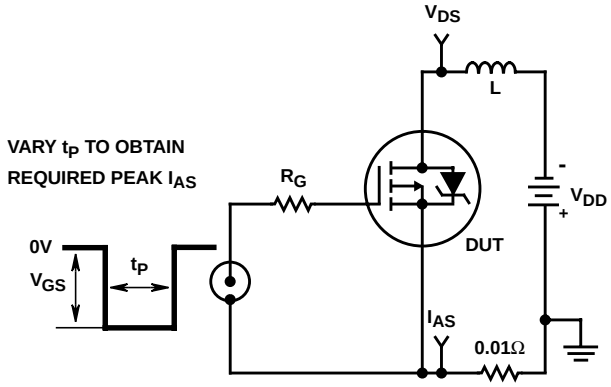


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

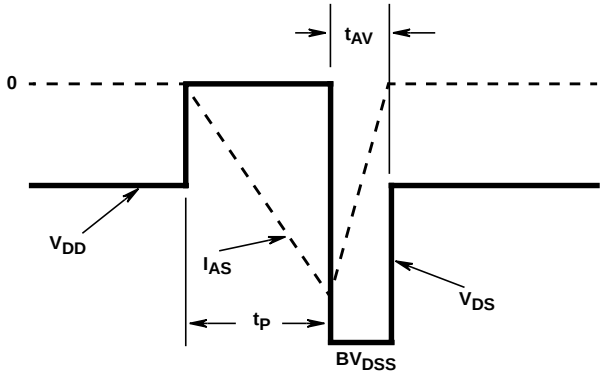


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

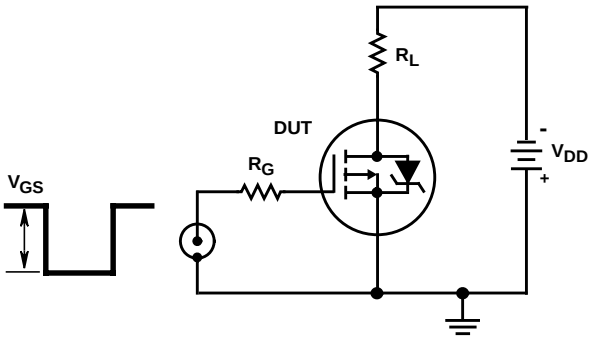


FIGURE 16. SWITCHING TIME TEST CIRCUIT

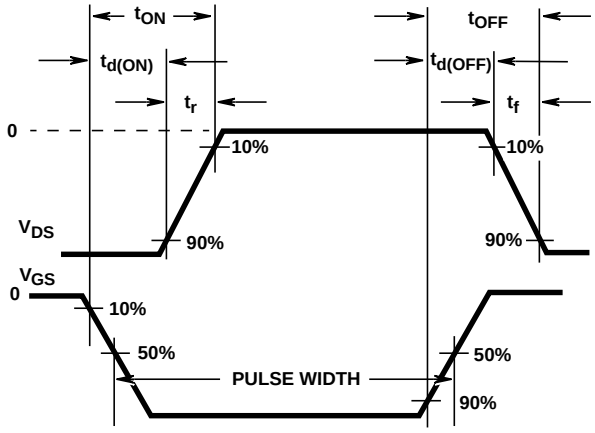


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

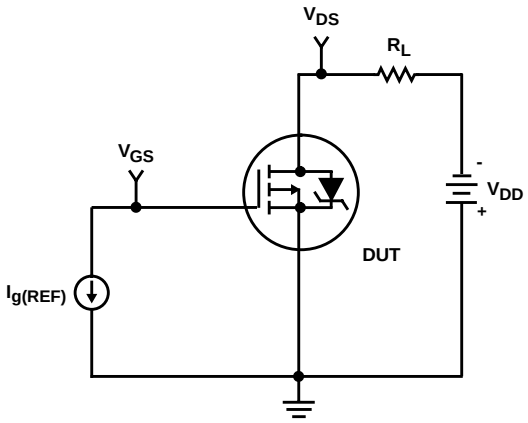


FIGURE 18. GATE CHARGE TEST CIRCUIT

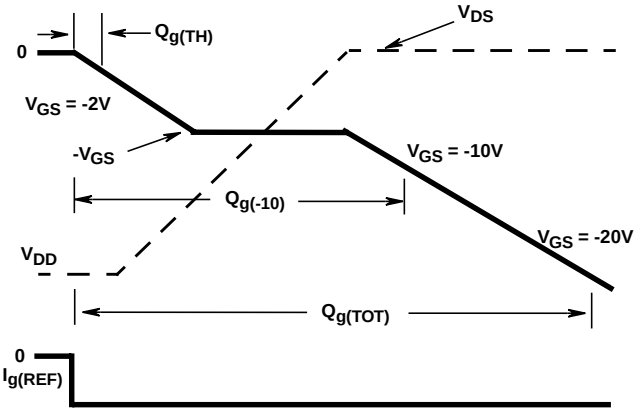


FIGURE 19. GATE CHARGE WAVEFORMS

PSPICE Electrical Model

```
.SUBCKT RFP15P05  2  1  3        REV 9/06/94

CA 12 8 1.6e-9
CB 15 14 1.47e-9
CIN 6 8 1.09e-9

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -73.0
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 6.73e-9
LSOURCE 3 7 6.69e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 63.6e-3
RGATE 9 20 7.37
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 46.5e-3
RVTO 18 19 RVTOMOD 1

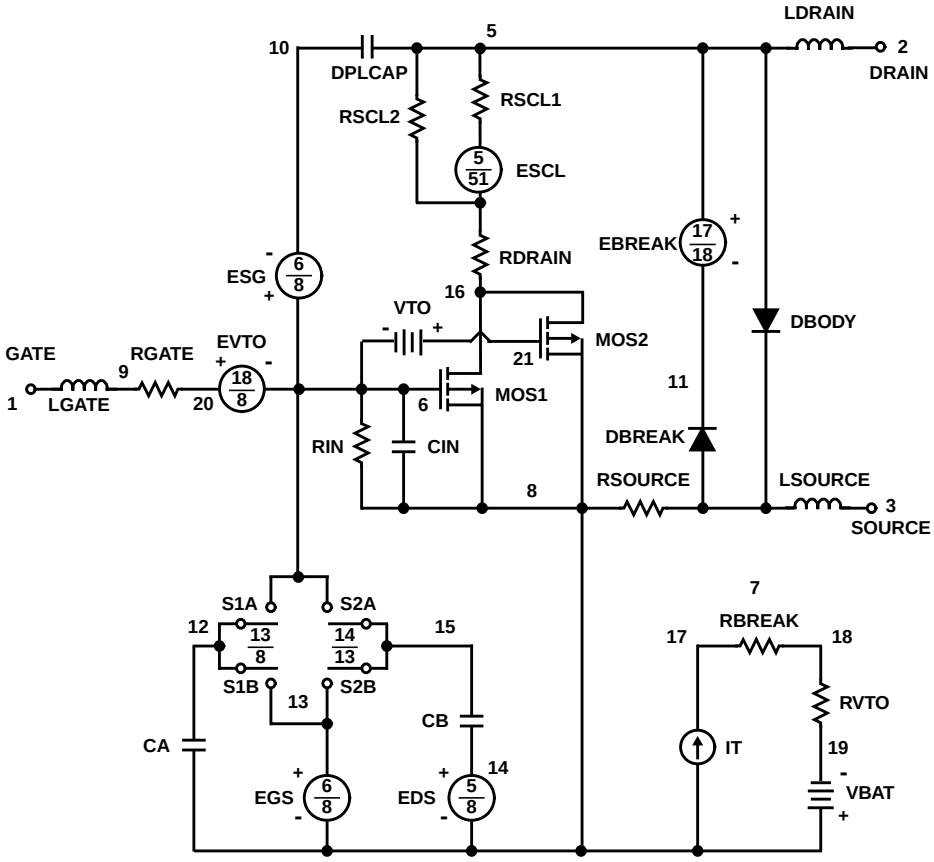
S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.65

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/35,4))}

.MODEL DBDMOD D (IS = 1.27e-13 RS = 1.62e-2 TRS1 = 1.35e-3 TRS2 = -4.33e-6 CJO = 1.25e-9 TT = 7.97e-8)
.MODEL DBKMOD D (RS = 2.54e-1 TRS1 = 4.54e-3 TRS2 = -1.12e-5)
.MODEL DPLCAPMOD D (CJO = 285e-12 IS = 1e-30 N = 10)
.MODEL MOSMOD PMOS (VTO = -3.78 KP = 6.97 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 9.15e-4 TC2 = -4.0e-7)
.MODEL RDSMOD RES (TC1 = 5.47e-3 TC2 = 1.37e-5)
.MODEL RSCLMOD RES (TC1 = 1.9e-3 TC2 = -7.5e-6)
.MODEL RVTOMOD RES (TC1 = -3.71e-3 TC2 = -2.41e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 3.65 VOFF = 1.65)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.65 VOFF = 3.65)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.60 VOFF = -4.40)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.40 VOFF = 0.60)

.ENDS
```



NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.