1.0 General Description

The AMIS-42665 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus and may be used in both 12V and 24V systems. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The AMIS-42665 is a new addition to the CAN high-speed transceiver family and offers the following additional features:

- Ideal passive behavior when supply voltage is removed
- Wake-up over bus
- Extremely low current standby mode

Due to the wide common-mode voltage range of the receiver inputs, the AMIS-42665 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

2.0 Key Features

- Compatible with the ISO 11898 standard
- High speed (up to 1Mbaud)
- Ideally suited for 12V and 24V industrial and automotive applications
- Extremely low current standby mode with wake-up via the bus
- Low EME common-mode-choke is no longer required
- Differential receiver with wide common-mode range (+/- 35V) for high EMS
- No disturbance of the bus lines with an un-powered node
- Transmit data (TxD) dominant time-out function
- Thermal protection
- Bus pins protected against transients in an automotive environment
- Power down mode in which the transmitter is disabled
- Short circuit proof to supply voltage and ground
- Logic level inputs compatible with 3.3V devices
- Voltage source for via Vsplit pin for stabilizing the recessive bus level (further EMC improvement)

3.0 Technical Characteristics

Table 1: Technical Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Power supply voltage		4.75	5.25	V
V_{STB}	DC voltage at pin STB		-0.3	V_{CC}	V
V_{TxD}	DC voltage at pin TxD		-0.3	V_{CC}	V
V_{RxD}	DC voltage at pin RxD		-0.3	V_{CC}	V
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.25V$; no time limit	-35	+35	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.25V$; no time limit	-35	+35	V
V_{SPLIT}	DC voltage at pin V_{SPLIT}	$0 < V_{CC} < 5.25V$; no time limit	-35	+35	V
$V_{i(dif)(bus\_dom)}$	Differential bus output voltage in dominant state	$42.5\Omega < R_{LT} < 60\Omega$	1.5	3	V
CM-range	Input common-mode range for comparator	Guaranteed differential receiver threshold and leakage current	-35	+35	V
$V_{CM-peak}$	Common-mode peak	See Figure 8 and 9 (Note)	-500	500	mV
C_{load}	Load capacitance on IC outputs			15	pF
$t_{pd(rec-dom)}$	Propagation delay TxD to RxD	See Figure 7	70	230	ns
$t_{pd(dom-rec)}$	Propagation delay TxD to RxD	See Figure 7	100	245	ns
$V_{CM-step}$	Common-mode step	See Figure 8 and 9 (Note)	-150	150	mV
T_{junc}	Junction temperature		-40	150	°C

Notes: The parameters $V_{CM-peak}$ and $V_{CM-step}$ guarantee low electromagnetic emission.

4.0 Ordering Information

Marketing Name	Package	Temp. Range
AMIS42665AGA	SOIC 150 8 GREEN	-40°C…125°C

5.0 Block Diagram

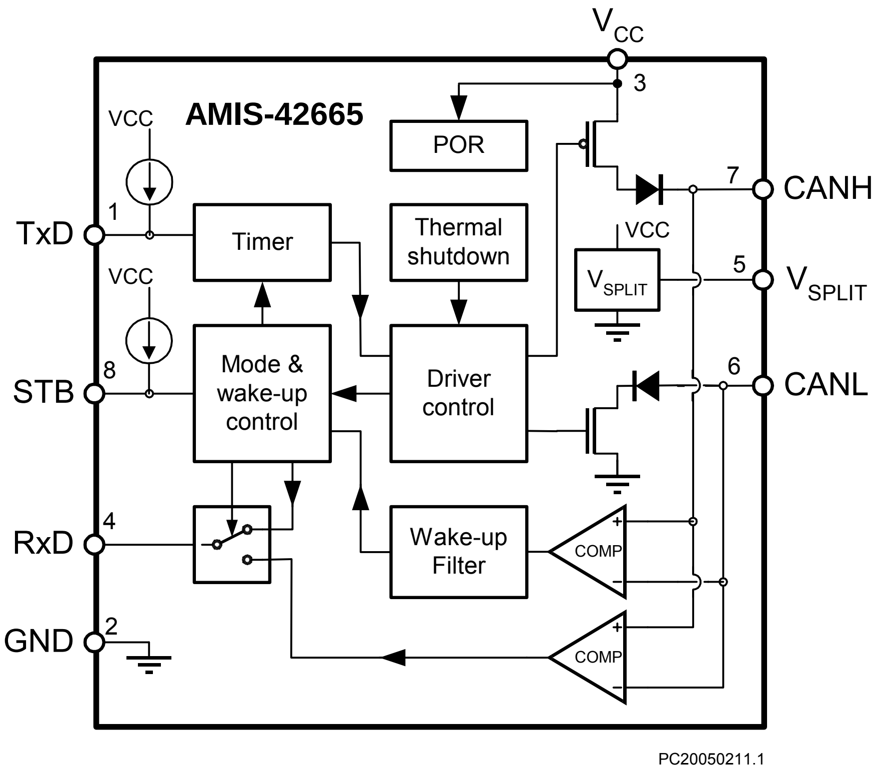


Figure 1: Block Diagram

6.0 Typical Application

6.1 Application Schematic

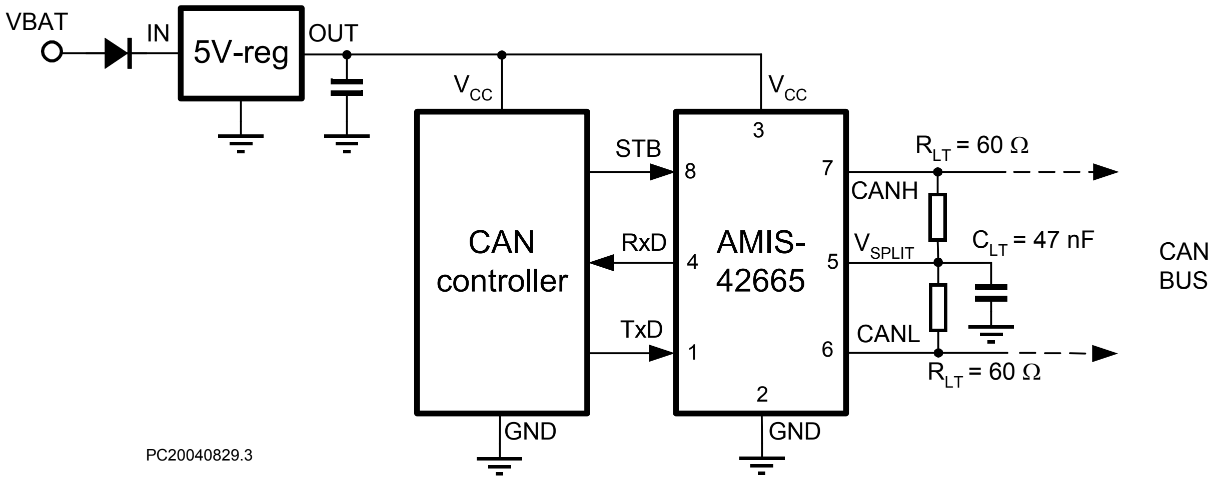


Figure 2: Application Diagram

6.2 Pin Description

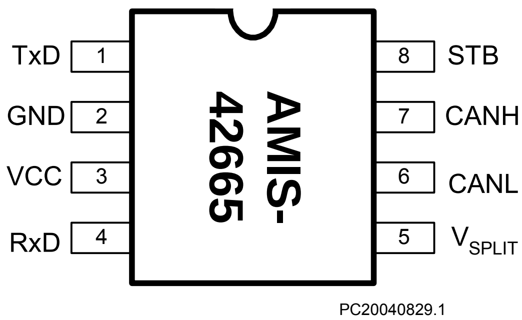


Figure 3: Pin Configuration

Table 2: Pinout

Pin	Name	Description
1	TxD	Transmit data input; low input => dominant driver; internal pull-up current
2	GND	Ground
3	V_{CC}	Supply voltage
4	RxD	Receive data output; dominant transmitter => low output
5	V_{SPLIT}	Common-mode stabilization output
6	CANL	LOW-level CAN bus line (low in dominant mode)
7	CANH	HIGH-level CAN bus line (high in dominant mode)
8	STB	Standby mode control input

7.0 Functional Description

7.1 Operating Modes

AMIS-42665 provides two modes of operation as illustrated in Table 3. These modes are selectable through pin STB.

Table 3: Operating Modes

Mode	Pin STB	Pin RXD	
		Low	High
Normal	Low	Bus dominant	Bus recessive
Standby	High	Wake-up request detected	No wake-up request detected

7.1.1 Normal Mode

In the normal mode, the transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimized to give extremely low EME.

7.1.2 Standby Mode

In standby mode both the transmitter and receiver are disabled and a very low-power differential receiver monitors the bus lines for CAN bus activity. The bus lines are terminated to ground and supply current is reduced to a minimum, typically 10µA. When a wake-up request is detected by the low-power differential receiver, the signal is first filtered and then verified as a valid wake signal after a time period of t_{BUS}, the RxD pin is driven low by the transceiver to inform the controller of the wake-up request.

7.2 Split Circuit

The V_{SPLIT} pin is operational only in normal mode. In standby mode this pin is floating. The V_{SPLIT} is connected as shown in Figure 2 and its purpose is to provide a stabilized DC voltage of 0.5 x V_{CC} to the bus avoiding possible steps in the common-mode signal therefore reducing EME. These unwanted steps could be caused by an un-powered node on the network with excessive leakage current from the bus that shifts the recessive voltage from its nominal 0.5 x V_{CC} voltage.

7.3 Wake-up

Once a valid wake-up (dominant state longer than t_{BUS}) has been received during the standby mode the RxD pin is driven low.

7.4 Over-temperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 160°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off-state resets when pin TxD goes high. The thermal protection circuit is particularly needed when a bus line short circuits.

7.5 TxD dominant Time-out Function

A TxD dominant time-out timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication) if pin TxD is forced permanently low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the low-level on pin TxD exceeds the internal timer value t_{dom}, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pin TxD.

7.6 Fail-safe Features

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

The pins CANH and CANL are protected from automotive electrical transients (according to ISO 7637; see Figure 4). Pins TxD and STB are pulled high internally should the input become disconnected. Pins TxD, STB and RxD will be floating, preventing reverse supply should the V_{CC} supply be removed.

8.0 Electrical Characteristics

8.1 Definitions

All voltages are referenced to GND (pin 2). Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

8.2 Absolute Maximum Ratings

Stresses above those listed in the following table may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may effect device reliability.

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage		-0.3	+7	V
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.25V$; no time limit	-50	+50	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.25V$; no time limit	-50	+50	V
V_{SPLIT}	DC voltage at pin VSPLIT	$0 < V_{CC} < 5.25V$; no time limit	-50	+50	V
V_{TxD}	DC voltage at pin TxD		-0.3	V_{CC} + 0.3	V
V_{RxD}	DC voltage at pin RxD		-0.3	V_{CC} + 0.3	V
V_{STB}	DC voltage at pin STB		-0.3	V_{CC} + 0.3	V
$V_{tran(CANH)}$	Transient voltage at pin CANH	Note 1	-300	+300	V
$V_{tran(CANL)}$	Transient voltage at pin CANL	Note 1	-300	+300	V
$V_{tran(VSPLIT)}$	Transient voltage at pin VSPLIT	Note 1	-300	+300	V
$V_{esd(CANL/CANH/VSPLIT)}$	Electrostatic discharge voltage at CANH and CANL pin	Note 2 Note 4	-8 -500	+8 +500	kV V
V_{esd}	Electrostatic discharge voltage at all other pins	Note 2 Note 4	-4 -500	+ 4 +500	kV V
Latch-up	Static latch-up at all pins	Note 3		100	mA
T_{stg}	Storage temperature		-55	+155	°C
T_{amb}	Ambient temperature		-40	+125	°C
T_{junc}	Maximum junction temperature		-40	+170	°C

Notes
1) Applied transient waveforms in accordance with ISO 7637 part 3, test pulses 1, 2, 3a, and 3b (see Figure 4).
2) Standardized human body model electrostatic discharge (ESD) pulses in accordance to MIL883 method 3015.7.
3) Static latch-up immunity: Static latch-up protection level when tested according to EIA/JESD78.
4) Standardized charged device model ESD pulses when tested according to EOS/ESD DS5.3-1993.

8.3 Thermal Characteristics

Table 5: Thermal Characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(vj-a)}$	Thermal resistance from junction to ambient in SO8 package	In free air	145	K/W
$R_{th(vj-s)}$	Thermal resistance from junction to substrate of bare die	In free air	45	K/W

8.4 Characteristics

V_{CC} = 4.75 to 5.25V; T_{junc} = -40 to +150°C; R_{LT} =60Ω unless specified otherwise.

Table 6: Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply (pin V_{CC})						
I_{CC}	Supply current	Dominant; V_{TxD} =0V Recessive; V_{TxD} =V_{CC}		45 4	65 8	mA mA
I_{CCS}	Supply current in sleep mode	$T_{junc,max}$ = 100°C		10	15	µA
I_{CCS}	Supply current in sleep mode	$T_{junc,max}$ = 150°C		10	20	µA
Transmitter Data Input (pin TxD)						
V_{IH}	High-level input voltage	Output recessive	2.0	-	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	Output dominant	-0.3	-	+0.8	V
I_{IH}	High-level input current	V_{TxD} =V_{CC}	-5	0	+5	µA
I_{IL}	Low-level input current	V_{TxD} =0V	-75	-200	-350	µA
C_i	Input capacitance	Not tested	-	5	10	pF
Transmitter Mode Select (pin STB)						
V_{IH}	High-level input voltage	Standby mode	2.0	-	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	Normal mode	-0.3	-	+0.8	V
I_{IH}	High-level input current	V_{STB} =V_{CC}	-5	0	+5	µA
I_{IL}	Low-level input current	V_{STB} =0V	-1	-4	-10	µA
C_i	Input capacitance	Not tested	-	5	10	pF
Receiver Data Output (pin RxD)						
V_{OH}	High-level output voltage	I_{RXD} = -10mA	0.6 x V_{CC}		0.75 x V_{CC}	V
V_{OL}	Low-level output voltage	I_{RXD} = 5mA		0.25	0.45	V
I_{oh}	High-level output current	V_o=0.7 x V_{CC}	-5	-10	-15	mA
I_{ol}	Low-level output current	V_o=0.3 x V_{CC}	5	10	15	mA
Bus Lines (pins CANH and CANL)						
$V_{o(reces)\ (norm)}$	Recessive bus voltage	V_{TxD} = V_{CC}; no load normal mode	2.0	2.5	3.0	V
$V_{o(reces)\ (stby)}$	Recessive bus voltage	V_{TxD} = V_{CC}; no load standby mode	-100	0	100	mV
$I_{o(reces)\ (CANH)}$	Recessive output current at pin CANH	-35V <V_{CANH}< +35V; 0V <V_{CC} < 5.25V	-2.5	-	+2.5	mA
$I_{o(reces)\ (CANL)}$	Recessive output current at pin CANL	-35V <V_{CANL} < +35V; 0V <V_{CC} < 5.25V	-2.5	-	+2.5	mA
$V_{o(dom)\ (CANH)}$	Dominant output voltage at pin CANH	V_{TxD} = 0V	3.0	3.6	4.25	V
$V_{o(dom)\ (CANL)}$	Dominant output voltage at pin CANL	V_{TxD} = 0V	0. 5	1.4	1.75	V
$V_{i(dif)\ (bus\_dom)}$	Differential bus input voltage (V_{CANH} - V_{CANL})	V_{TxD} = 0V; dominant; 42.5Ω < R_{LT} < 60Ω	1.5	2.25	3.0	V
$V_{i(dif)\ (bus\_rec)}$	Differential bus input voltage (V_{CANH} - V_{CANL})	V_{TxD} = V_{CC}; recessive; no load	-120	0	+50	mV
$I_{o(sc)\ (CANH)}$	Short circuit output current at pin CANH	V_{CANH} = 0V; V_{TxD} =0V	-45	-70	-120	mA
$I_{o(sc)\ (CANL)}$	Short circuit output current at pin CANL	V_{CANL} = 36V; V_{TxD} =0V	45	70	120	mA
$V_{i(dif)\ (th)}$	Differential receiver threshold voltage (see Figure 5)	-5V <V_{CANL} < +12V; -5V <V_{CANH} < +12V;	0.5	0.7	0.9	V
$V_{ihcm(dif)\ (th)}$	Differential receiver threshold voltage for high common-mode (see Figure 5)	-35V <V_{CANL} < +35V; -35V <V_{CANH} < +35V;	0.30	0.7	1.05	V
$V_{i(dif)\ (hys)}$	Differential receiver input voltage hysteresis (see Figure 5)	-35V <V_{CANL} < +35V; -35V <V_{CANH} < +35V;	50	70	100	mV
$R_{i(cm)\ (CANH)}$	Common-mode input resistance at pin CANH		15	26	37	KΩ
$R_{i(cm)\ (CANL)}$	Common-mode input resistance at pin CANL		15	26	37	KΩ
$R_{i(cm)\ (m)}$	Matching between pin CANH and pin CANL common mode input resistance	V_{CANH} =V_{CANL}	-3	0	+3	%
$R_{i(dif)}$	Differential input resistance		25	50	75	KΩ
$C_{i(CANH)}$	Input capacitance at pin CANH	V_{TxD} = V_{CC}; not tested		7.5	20	pF
$C_{i(CANL)}$	Input capacitance at pin CANL	V_{TxD} = V_{CC}; not tested		7.5	20	pF
$C_{i(dif)}$	Differential input capacitance	V_{TxD} = V_{CC}; not tested		3.75	10	pF
$I_{LI(CANH)}$	Input leakage current at pin CANH	V_{CC} = 0V; V_{CANH} = 5V	-5	0	+5	µA
$I_{LI(CANL)}$	Input leakage current at pin CANL	V_{CC} = 0V; V_{CANL} = 5V	-5	0	+5	µA
$V_{CM-peak}$	Common-mode peak during transition from dom → rec or rec → dom	See Figure 8 and 9	-500		500	mV
$V_{CM-step}$	Difference in common-mode between dominant and recessive state	See Figure 8 and 9	-150		150	mV

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Common-mode Stabilization (pin V_{SPLIT})						
V_{SPLIT}	Reference output voltage at pin V_{SPLIT}	Normal mode; $-500\mu A < I_{SPLIT} < 500\mu A$	0.3 x V_{CC}	-	0.7 x V_{CC}	
$I_{SPLIT(i)}$	V_{SPLIT} leakage current	Standby mode	-5		+5	µA
$I_{SPLIT(lim)}$	V_{SPLIT} limitation current	Normal mode	-3		+3	mA
Power-on-Reset						
PORL	POR level	CANH, CANL, V_{ref} in tri-state below POR level	2.2	3.5	4.7	V
Thermal Shutdown						
$T_{j(sd)}$	Shutdown junction temperature		150	160	180	°C
Timing Characteristics (see Figure 6 and 7)						
$t_{d(TxD\text{-}BUSon)}$	Delay TXD to bus active	C_l = 100pF between CANH to CANL	40	85	105	ns
$t_{d(TxD\text{-}BUSoff)}$	Delay TXD to bus inactive	C_l = 100pF between CANH to CANL	30	60	105	ns
$t_{d(BUSon\text{-}RXD)}$	Delay bus active to RXD	C_{rxd} = 15pF	25	55	105	ns
$t_{d(BUSoff\text{-}RXD)}$	Delay bus inactive to RXD	C_{rxd} = 15pF	65	100	130	ns
$t_{pd(rec\text{-}dom)}$	Propagation delay TXD to RXD from recessive to dominant	C_l = 100pF between CANH to CANL	70		230	ns
$t_{d(dom\text{-}rec)}$	Propagation delay TXD to RXD from dominant to recessive	C_l = 100pF between CANH to CANL	100		245	ns
$t_{d(stb\text{-}nm)}$	Delay standby mode to normal mode		5	7.5	10	µs
t_{dbus}	Dominant time for wake-up via bus		0.75	2.5	5	µs
$t_{dom(TxD)}$	TxD dominant time for time out	V_{TxD} = 0V	300	600	1000	µs

8.5 Measurement Set-ups and Definitions

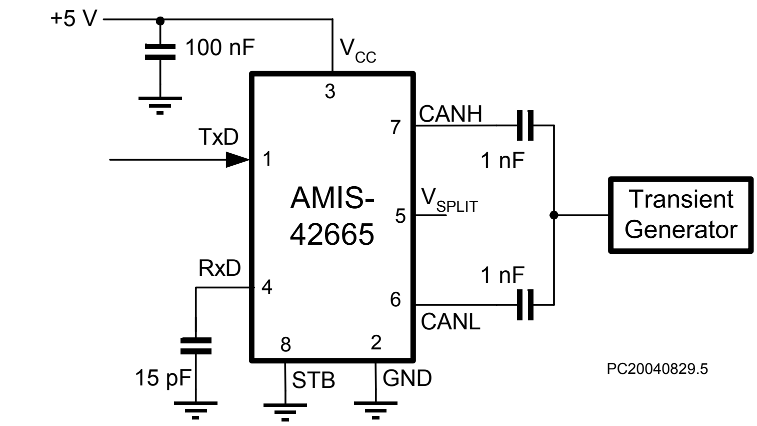


Figure 4: Test Circuit for Automotive Transients

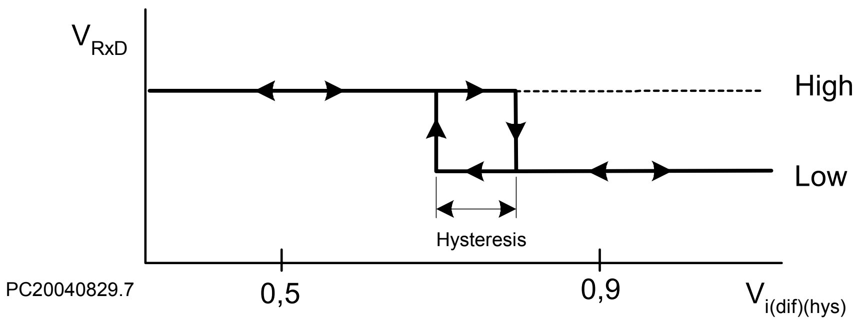


Figure 5: Hysteresis of the Receiver

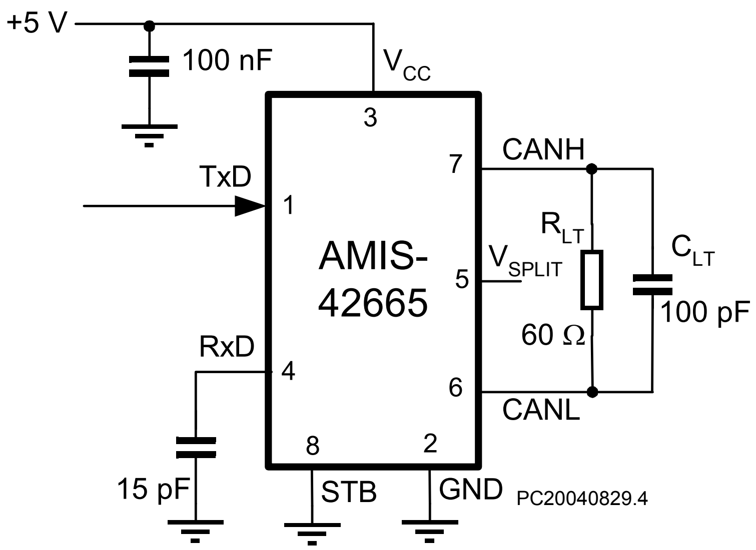


Figure 6: Test Circuit for Timing Characteristics

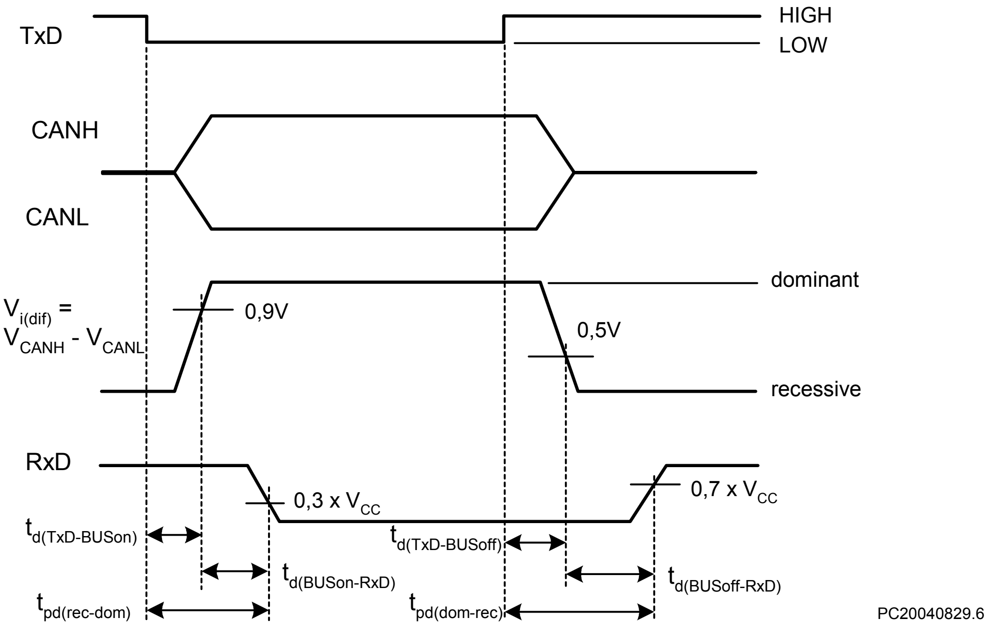


Figure 7 – Timing Diagram for AC Characteristics

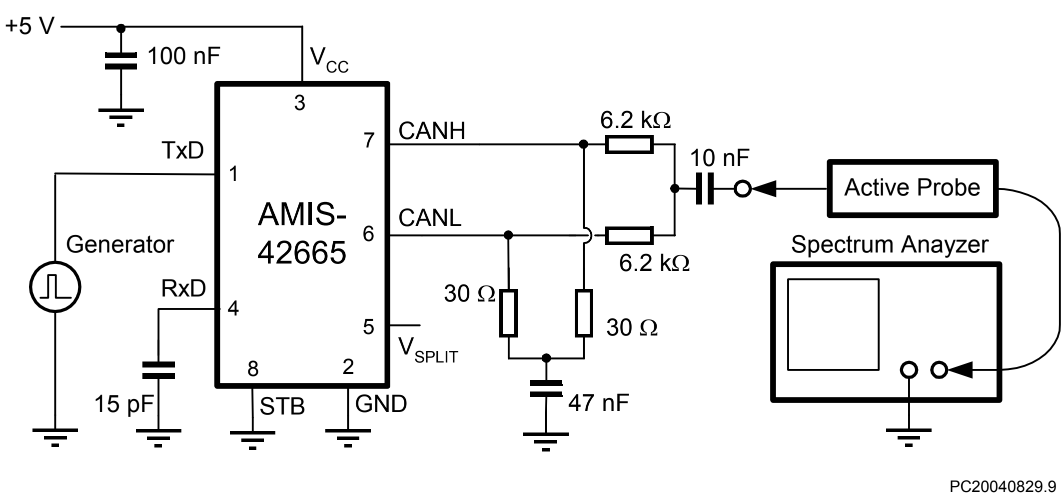


Figure 8: Basic Test Setup for Electromagnetic Measurement

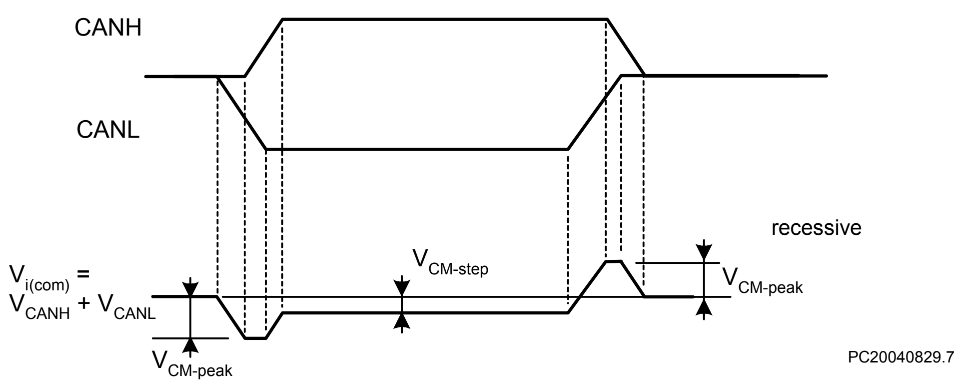
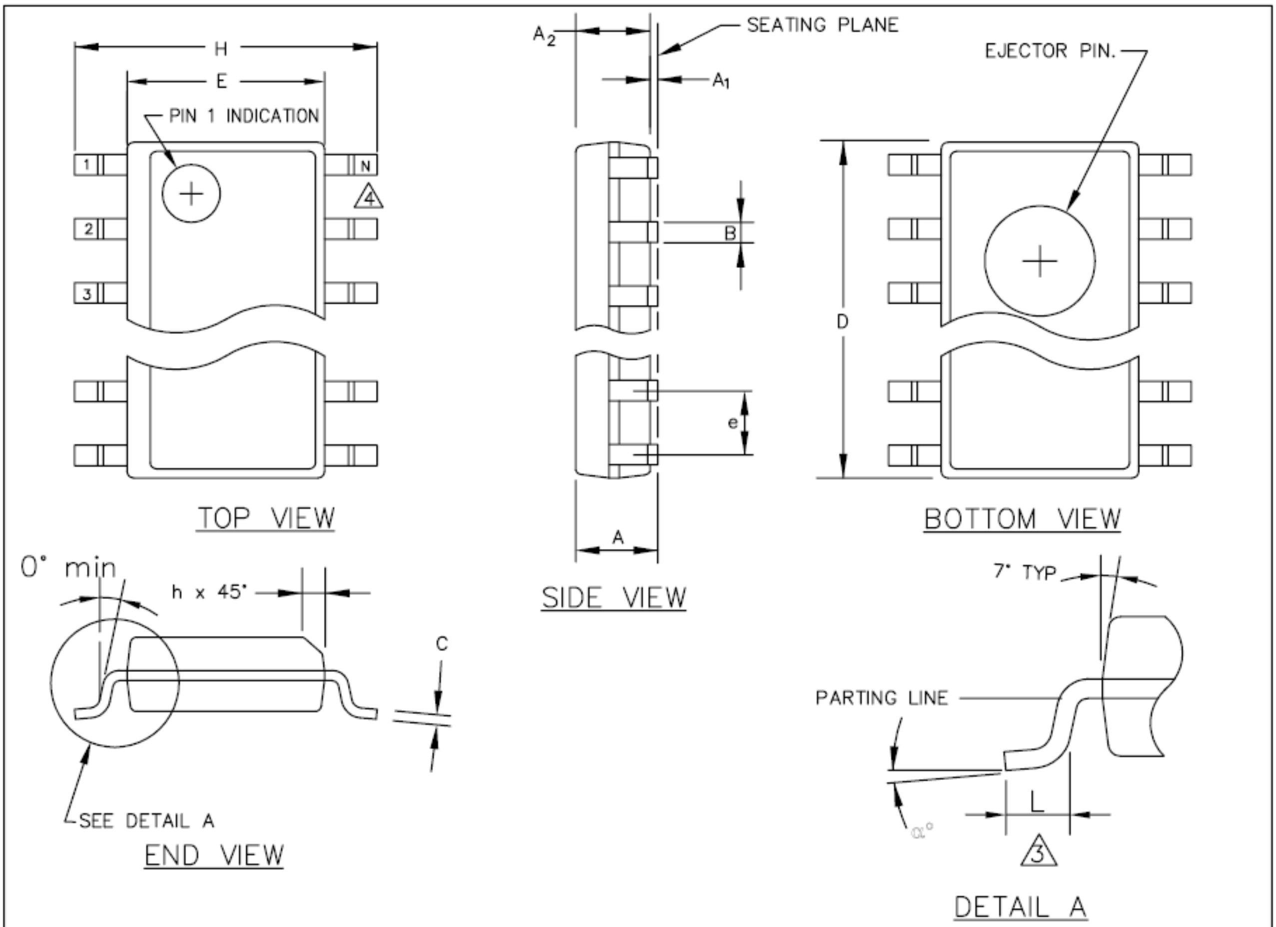


Figure 9: Common-mode Voltage Peaks (see Measurement Setup Figure 8)

9.0 Package Outline

SOIC-8: Plastic small outline; 8 leads; body width 150 mil. AMIS reference: SOIC150 8 150 G



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	.061	.064	.068	
A_1	.004	.006	0.010	
A_2	.055	.058	.061	
B	.0138	.016	.020	
C	.0075	.008	.0098	
D	SEE VARIATIONS			1
E	.150	.155	.157	
e	.050 BSC			
H	.230	.236	.244	
h	.010	.013	.016	
L	.016	.025	.035	
N	SEE VARIATIONS			2
α°	0°	5°	8°	

VARIATIONS				
	1			2
	D			N
NOTE	MIN.	NOM.	MAX.	
AA	.189	.194	.196	8
AB	.337	.342	.344	14
AC	.386	.391	.393	16

NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M – 1982.
3. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
4. "N" IS THE NUMBER OF TERMINAL POSITIONS.
5. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
6. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
7. CONTROLLING DIMENSION: INCHES.

Drawn: PJ 10/28/03
CAD Dwg. No. 6000209.DWG
Ref Dwg. No.
Drawing Number\CAD File: 6000209
Rev. D
Scale:
Sheet

SOIC150
8, 14, 16 LEAD

AMI SEMICONDUCTOR, Inc.
2300 Buckskin Rd., Pocatello, Idaho 83201

10.0 Soldering

10.1 Introduction to Soldering Surface Mount Packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in the AMIS “Data Handbook IC26; Integrated Circuit Packages” (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

10.2 Reflow Soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250°C. The top-surface temperature of the packages should preferably be kept below 230°C.

10.3 Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems. To overcome these problems the double-wave soldering method was specifically developed. If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

- For packages with leads on two sides and a pitch (e):
  - Larger than or equal to 1.27mm, the footprint longitudinal axis is preferred to be parallel to the transport direction of the printed circuit board;
  - Smaller than 1.27mm, the footprint longitudinal axis must be parallel to the transport direction of the printed circuit board. The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45º angle to the transport direction of the printed circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is four seconds at 250°C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

10.4 Manual Soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C. When using a dedicated tool, all other leads can be soldered in one operation within two to five seconds between 270 and 320°C.

Package	Soldering Method	
	Wave	Reflow(1)
BGA, SQFP	Not suitable	Suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	Not suitable (2)	Suitable
PLCC (3) , SO, SOJ	Suitable	Suitable
LQFP, QFP, TQFP	Not recommended (3)(4)	Suitable
SSOP, TSSOP, VSO	Not recommended (5)	Suitable

Notes
1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5mm.

11.0 Company or Product Inquiries

For more information about AMI Semiconductor, our technology and our product, visit our website at: http://www.amis.com

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