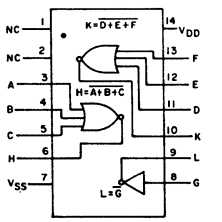
Digital Integrated Circuits

Monolithic Silicon

CD4000A,CD4001A CD4002A,CD4025A

Types



CD4000A

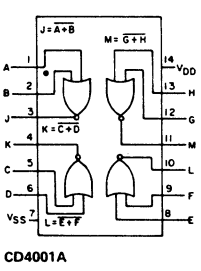
COS/MOS NOR Gates (Positive Logic)

Special Features

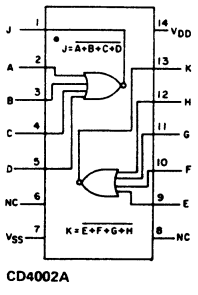
- Medium speed operation. . . . . $t_{PHL} = t_{PLH} = 25$ ns (typ.) at $C_L = 15$ pF
- Low "high"- and "low"-level output impedance. . . . . 500Ω and 200Ω (typ), respectively at $V_{DD} - V_{SS} = 10$ V

Dual 3 Input plus Inverter	CD4000AD, CD4000AE, CD4000AF, CD4000AK
Quad 2 Input	CD4001AD, CD4001AE, CD4001AF, CD4001AK
Dual 4 Input	CD4002AD, CD4002AE, CD4002AF, CD4002AK
Triple 3 Input	CD4025AD, CD4025AE, CD4025AF, CD4025AK

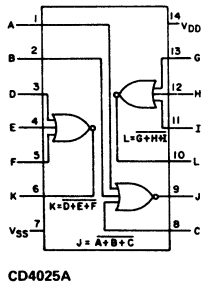
The combination of these devices and the RCA NAND positive logic gate types CD4011A, CD4012A, and CD4023A can account for appreciable package-count savings in various logic function configurations.



CD4001A



CD4002A



CD4025A

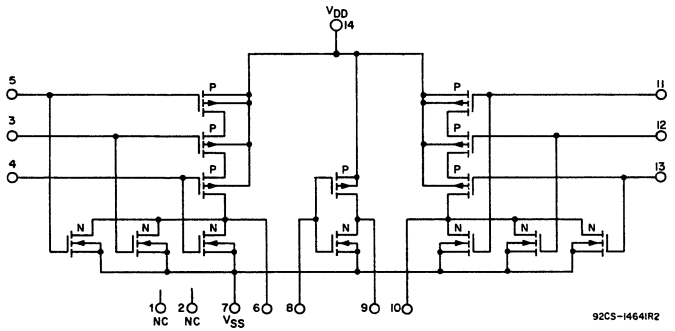


Fig.1.1—Schematic diagram for type CD4000A.

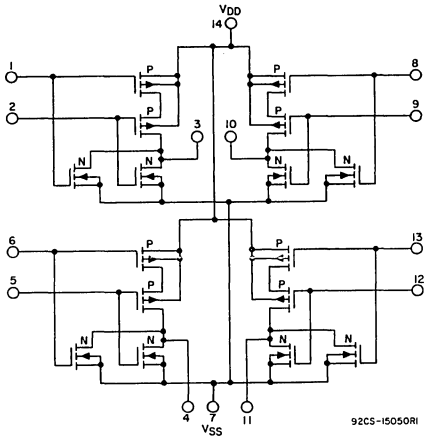


Fig.1.2–Schematic diagram for type CD4001A.

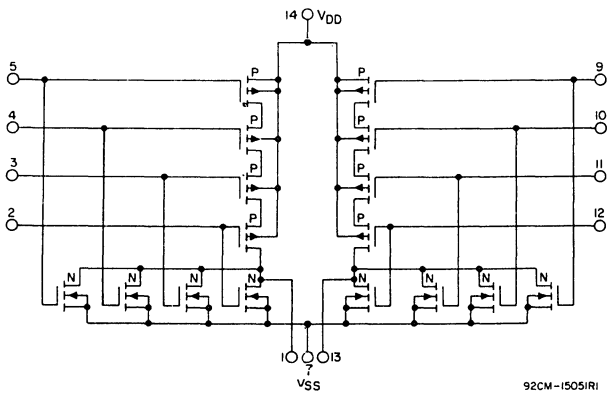


Fig.1.3–Schematic diagram for type CD4002A.

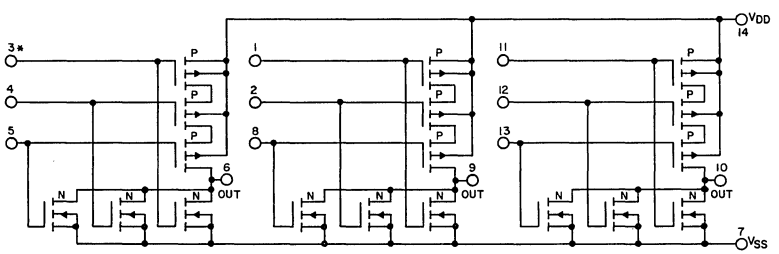


Fig.1.4–Schematic diagram for type CD4025A.

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . . $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) . . . . . **3 to 15 V)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4000AD,CD4001AD,CD4002AD,CD4025AD, CD4000AK,CD4001AK,CD4002AK,CD4025AK, CD4000AF,CD4001AF,CD4002AF,CD4025AF									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS
				−55°C			25°C			125°C				Fig. No.
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Quiescent Device Current	I_L		5	–	–	0.05	–	0.001	0.05	–	–	3	μA	
			10	–	–	0.1	–	0.001	0.1	–	–	6		
Quiescent Device Dissipation/Package	P_D		5	–	–	0.25	–	0.005	0.25	–	–	15	μW	
			10	–	–	1	–	0.01	1	–	–	60		
Output Voltage: Low-Level	V_{OL}	$V_I=V_{DD}$ $I_O=0A$	5	–	–	0.01	–	0	0.01	–	–	0.05	V	15 16
			10	–	–	0.01	–	0	0.01	–	–	0.05		
High-Level	V_{OH}	$V_I=V_{SS}$ $I_O=0A$	5	4.99	–	–	4.99	5	–	4.95	–	–	V	17
			10	9.99	–	–	9.99	10	–	9.95	–	–		
Noise Immunity (Any Input) *For Definition, See Appendix*	V_{NL}	$I_O=0$ 3.6	5	1.5	–	–	1.5	2.25	–	1.4	–	–	V	–
		7.2	10	3	–	–	3	4.5	–	2.9	–	–		
	V_{NH}	0.95	5	1.4	–	–	1.5	2.25	–	1.5	–	–	V	–
		2.9	10	2.9	–	–	3	4.5	–	3	–	–		
Output Drive Current: N-Channel	I_{DN}	$V_I=V_{DD}$ 0.4▲	5	0.5	–	–	0.40	1	–	0.28	–	–	mA	18 1.10♦
		0.5	10	1.1	–	–	0.9	2.5	–	0.65	–	–		
P-Channel	I_{DP}	$V_I=V_{SS}$ 2.5≠	5	-0.62	–	–	-0.5	-2	–	-0.35	–	–	mA	19 1.11♦
		9.5	10	-0.62	–	–	-0.5	-1	–	-0.35	–	–		
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA	–

▲ Maximum noise-free low-level Bipolar output voltage.
≠ Minimum noise-free high-level Bipolar output voltage.
♦ See Appendix.

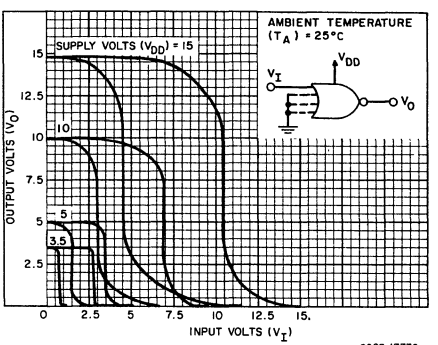


Fig. 1.5—Min. & max. voltage transfer characteristics.

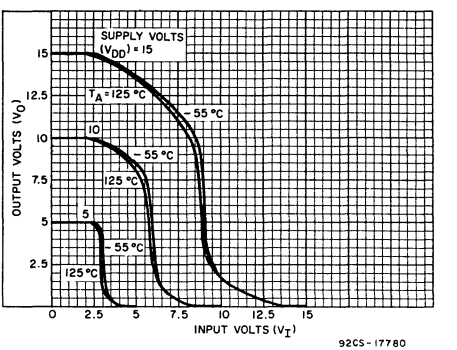


Fig. 1.6—Typ. voltage transfer characteristics as a function of temp.

STATIC ELECTRICAL CHARACTERISTICS (All inputs ..... $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4000AE, CD4001AE, CD4002AE, CD4025AE									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS
		V_O Volts		V_{DD} Volts	−40°C Min.	−40°C Typ.	−40°C Max.	25°C Min.	25°C Typ.	25°C Max.	85°C Min.	85°C Typ.	85°C Max.		Fig. No.
Quiescent Device Current	I_L			5	–	–	0.5	–	0.005	0.5	–	–	15	μA	
				10	–	–	5	–	0.005	5	–	–	30		
Quiescent Device Dissipation/Package	P_D			5	–	–	2.5	–	0.025	2.5	–	–	75	μW	
				10	–	–	50	–	0.05	50	–	–	300		
Output Voltage: Low-Level	V_{OL}	$V_I=V_{DD}$ $I_O=0A$		5	–	–	0.01	–	0	0.01	–	–	0.05	V	1.5, 1.6
				10	–	–	0.01	–	0	0.01	–	–	0.05		
High-Level	V_{OH}	$V_I=V_{SS}$ $I_O=0A$		5	4.99	–	–	4.99	5	–	4.95	–	–	V	1.7
				10	9.99	–	–	9.99	10	–	9.95	–			
Noise Immunity (Any Input) *For Definition, See Appendix*	V_{NL}	$I_O=0$	3.6	5	1.5		–	1.5	2.25		1.4			V	–
			7.2	10	3			3	4.5		2.9				
	V_{NH}		0.95	5	1.4	–		1.5	2.25		1.5			V	–
			2.9	10	2.9	–		3	4.5		3				
Output Drive Current: N-Channel	I_{DN}	$V_I=V_{DD}$	0.4▲	5	0.35	–	–	0.3	1	–	0.24	–	–	mA	1.8, 1.10 ♦
			0.5	10	0.72	–	–	0.6	2.5	–	0.48	–	–		
P-Channel	I_{DP}	$V_I=V_{SS}$	2.5≠	5	-0.35	–	–	-0.3	-2	–	-0.24	–	–	mA	1.9, 1.11 ♦
			9.5	10	-0.3	–	–	-0.25	-1	–	-0.2	–	–		
Input Current	I_I				–	–	–	–	10	–	–	–	–	pA	–

▲ Maximum noise-free low-level Bipolar output voltage.

≠ Minimum noise-free high-level Bipolar output voltage.

♦ See Appendix.

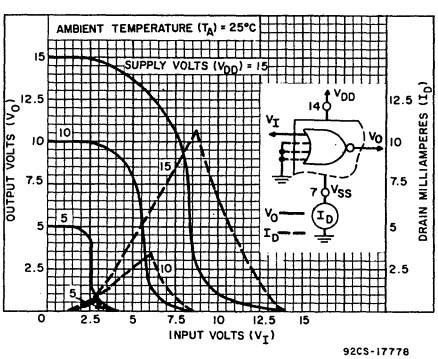


Fig. 1.7—Typ. current & voltage transfer characteristics.

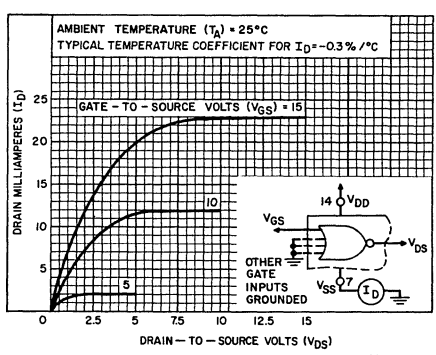


Fig. 1.8—Typ. n-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15pF, and input rise and fall times = 20 ns
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS
				CD4000AD, AF, AK CD4001AD, AF, AK CD4002AD, AF, AK CD4025AD, AF, AK			CD4000AE, CD4001AE CD4002AE, CD4025AE				
			V_{DD} (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig. No.
Propagation Delay Time: High-to-Low Level	t_{PHL}		5	–	35	50	–	35	80	ns	1.13
			10	–	25	40	–	25	55		
Low-to-High Level	t_{PLH}		5	–	35	95	–	35	120	ns	1.13
			10	–	25	45	–	25	65		
Transition Time: High-to-Low Level	t_{THL}		5	–	65	125	–	65	200	ns	1.14
			10	–	35	70	–	35	115		
Low-to-High Level	t_{TLH}		5	–	65	175	–	65	300	ns	1.14
			10	–	35	75	–	35	125		
Input Capacitance	C_I	Any Input		–	5	–	–	5	–	pF	–

DYNAMIC ELECTRICAL CHARACTERISTICS (Driving TTL, DTL) AT T_A = 25°C, $V_{DD}-V_{SS}$ = 5V, C_L = 5pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS						UNITS	TYPICAL CHARACTERISTICS CURVES
				CD4000AD, AF, AK CD4001AD, AF, AK CD4002AD, AF, AK CD4025AD, AF, AK			CD4000AE, CD4001AE CD4002AE, CD4025AE				
			Driving TTL, DTL	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig. No.
Propagation Delay Time: High-To-Low Level	t_{PHL}	R_L = 2kΩ	Med. Power	–	35	–	–	35	–	ns	1.15
		R_L = 20kΩ	Low Power	–	35	–	–	35	–		
Low-To-High Level	t_{PLH}	R_L = 2kΩ	Med. Power	–	15	–	–	15	–	ns	1.16
		R_L = 20kΩ	Low Power	–	20	–	–	20	–		
Transition Time	t_{THL} t_{TLH}	R_L = 2kΩ	Med. Power	–	40	–	–	40	–	ns	
		R_L = 20kΩ	Low Power	–	40	–	–	40	–		

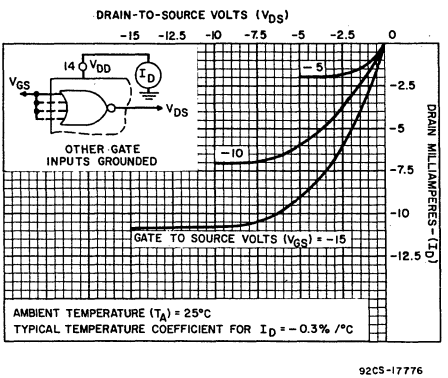


Fig. 1.9—Typ. p-channel drain characteristics.

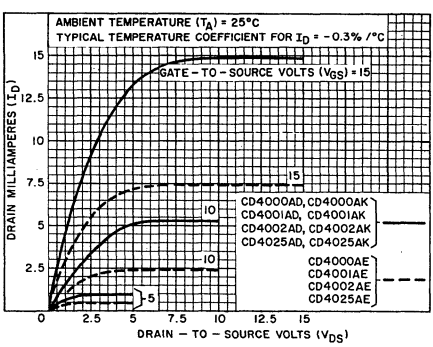


Fig. 1.10—Min. n-channel drain characteristics.

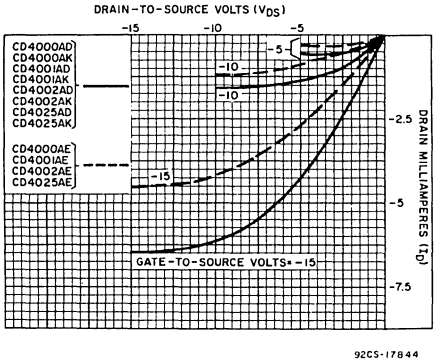


Fig. 1.11—Min. p-channel drain characteristics.

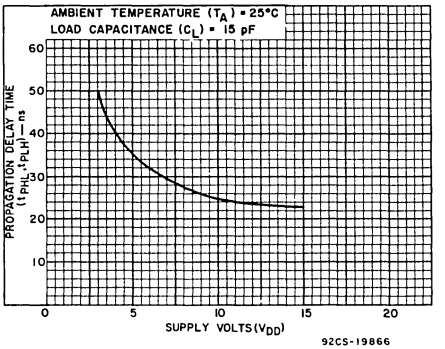


Fig. 1.12—Typ. propagation delay time vs. V_{DD}.

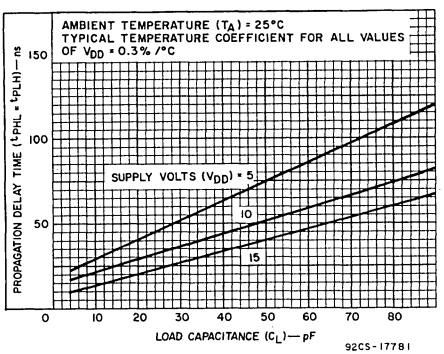


Fig. 1.13—Typ. propagation delay time vs. C_L.

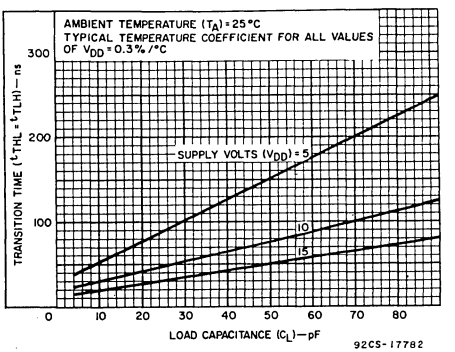


Fig. 1.14—Typ. transition time vs. C_L.

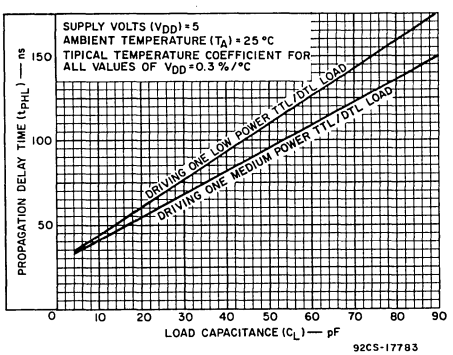


Fig. 1.15—Typ. low-level propagation delay time vs. C_L — driving TTL & DTL.

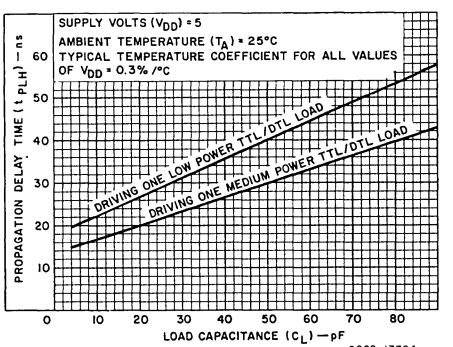


Fig. 1.16—Typ. high-level propagation delay time vs. C_L — driving TTL & DTL.

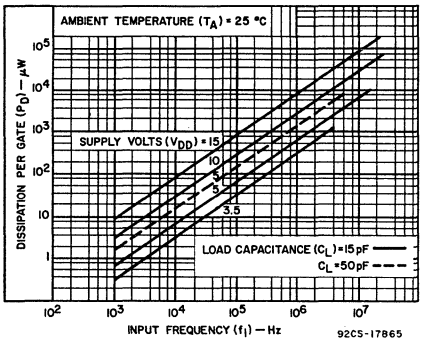
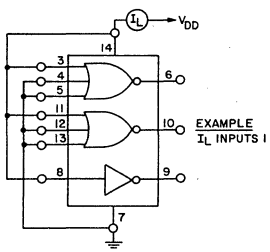
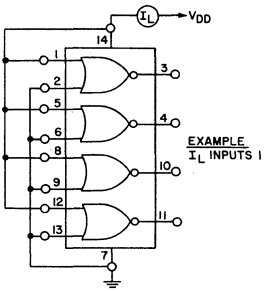


Fig.1.17 — Typ. dissipation characteristics.



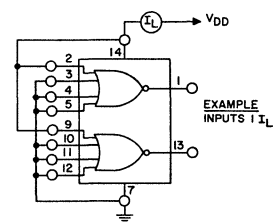
I_L MEASUREMENT	PIN CONNECTIONS TO V_{DD}	TO GND
INPUTS 1	3,11,8,14	4,5,7,12,13
INPUTS 2	4,12,8,14	3,5,7,11,13
INPUTS 3	5,13,8,14	3,4,7,11,12

Fig.1.18 — Quiescent device current test circuit for CD4000A.



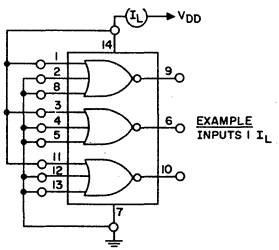
I_L MEASUREMENT	PIN CONNECTIONS TO V_{DD}	TO GND
INPUTS 1	1,5,8,12,14	2,6,7,9,13
INPUTS 2	2,6,9,13,14	1,5,7,8,12

Fig.1.19 — Quiescent device current test circuit for CD4001A.



I_L MEASUREMENT	PIN CONNECTIONS TO V_{DD}	TO GND
INPUTS 1	2,9,14	3,4,5,7,10,11,12
INPUTS 2	3,10,14	2,4,5,9,11,12
INPUTS 3	4,11,14	2,3,5,9,10,12
INPUTS 4	5,12,14	2,3,4,9,10,11

Fig.1.20 — Quiescent device current test circuit for CD4002A.



I_L MEASUREMENT	PIN CONNECTIONS TO V_{DD}	TO GND
INPUTS 1	1,3,11,14	2,4,5,7,8,12,13
INPUTS 2	2,4,12,14	1,3,5,7,8,11,13
INPUTS 3	8,5,13,14	1,2,3,4,7,11,12

Fig.1.21 — Quiescent device current test circuit for CD4025A.

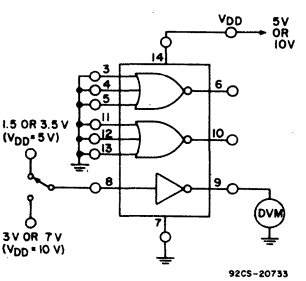


Fig.1.22 — Noise immunity test circuit for CD4000A.

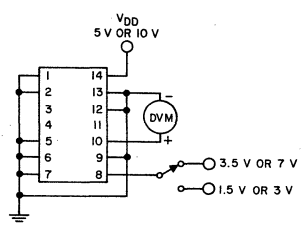


Fig.1.23 — Noise immunity test circuit for CD4001A.

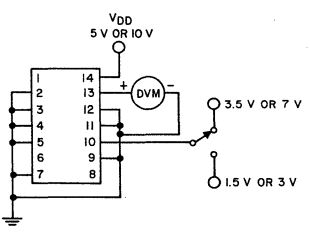


Fig.1.24 — Noise immunity test circuit for CD4002A.

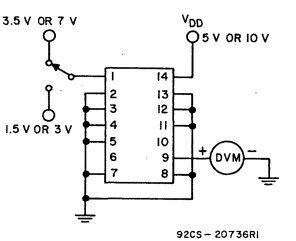


Fig.1.25 — Noise immunity test circuit for CD4025A.