PRODUCT / PROCESS CHANGE NOTIFICATION
PCN-000700
Date: APR-21-2021

Semtech Corporation, 200 Flynn Road, Camarillo CA 93012

Change Details

Part Number(s) Affected:	Customer Part Number(s) Affected: ☒ N/A
GN28L96-QFN-TR	

Description, Purpose and Effect of Change:

1) Minor digital logic change to prevent potential DDMI / ADC value corruption. This potential corruption can only happen under the specific condition where there is an I2C access of a DDMI / ADC value that is being written to by the internal DDMI controller logic at the same time.

   The issue has been corrected by using spare internal digital circuitry to ensure DDMI / ADC value writes happen coherently while asynchronous I2C events are happening.

2) Minor digital logic change to prevent potential LUT indexed multi-byte DAC value corruption. This potential corruption can only happen under the specific condition where there is an I2C access of a multi-byte DAC value that is being written to by the internal LUT controller logic at the same time.

   The issue has been corrected by using spare internal digital circuitry to ensure LUT / DAC value writes happen coherently while asynchronous I2C events are happening.

Change Classification	☐ **Major** ☒ **Minor**	**Impact to Form, Fit, Function**	☐ **Yes** ☒ **No**
Impact to Data Sheet	☐ **Yes** ☒ **No**	**New Revision or Date**	☒ **N/A**

Impact to Performance, Characteristics or Reliability:

No impact to performance, characteristics or reliability.

Implementation Date	**JUL-21-2021**	**Work Week**	**29**
Last Time Ship (LTS) **Of unchanged product**	**N/A**	**Affecting Lot No. / Serial No. (SN)**	**N/A**
Sample Availability	**N/A**	**Qualification Report Availability**	**N/A**

Supporting Documents for Change Validation/Attachments:

- Please see summary of changes on the next page

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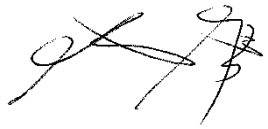
1) Changes to GN28L96 digital resolve issue where I2C double byte reads of ADC or DDMI values appear non-coherent because LSB and MSB don't refer to the same conversion.

- This affects all ADCs and DDMI values in current production silicon,
  - ADC values are only accessible with password level 2
  - Error rate of 4 per 10000 I2C reads when ADC conversion causes the most significant byte to change. Issue not otherwise detectable.
- Only the reported value is affected. Chip function is not affected
- Same test run on new fixed silicon finds no issue

2) Changes to GN28L96 digital resolve issue where LUT written multi-byte DAC values can temporarily appear non-coherent if the DAC location is accessed via I2C at the same time as the LUT controller writes to that location.

- It has not been possible to reproduce the issue on current production GN28L96 silicon.
  - APC_BIAS_LUT populated with values 0x0100 and 0x00FF recurring
  - External temperature input used to toggle between 2 LUT values at 100 Hz
  - Script to read back the register (APC_BIAS_SEED) that is populated by the LUT – any reading that is not 0x0100 or 0x00FF would be recorded as an error
  - No error was found for 20 Million I2C DAC reads
- Design have been able to simulate the issue and prove that new silicon resolves the issue in simulation.
  - Error reproduced by precisely controlling temperature and i2c read timing in simulation environment
- The test run on current production silicon has been run on the new silicon and shows no issue for over 20 million I2C reads of register APC_BIAS_SEED with LUT index changing at a rate of 100 changes per second
- Affected DAC registers:
  - ERC_MOD_SEED
  - APC_BIAS_SEED
  - APD_DAC_SEED
  - APD_RAMP_TGT
- Please note that these registers are only accessible with password level 2 access.

Issuing Authority		
Semtech Business Unit:	Signal Integrity Product Group (SIP)	
Semtech Contact Info:	Pedro Jr. Bernas Quality Assurance pbernas@semtech.com (289) 856-9326 x1162	
FOR FURTHER INFORMATION & WORLDWIDE SALES COVERAGE: http://www.semtech.com/contact/index.html#support		