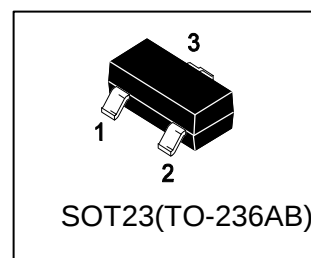


LP3401LT1G

30V P-Channel Enhancement-Mode MOSFET

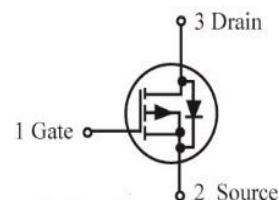
1. FEATURES

- $V_{DS} = -30V$
- $R_{DS(ON)} \leq 70m\Omega$ ($V_{GS} = -10V$)
- $R_{DS(ON)} \leq 80m\Omega$ ($V_{GS} = -4.5V$)
- $R_{DS(ON)} \leq 120m\Omega$ ($V_{GS} = -2.5V$)
- We declare that the material of product compliance with RoHS requirements and Halogen Free.



2. APPLICATIONS

- Advanced trench process technology
- High density cell design for ultra low on-resistance.



3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP3401LT1G	A1	3000/Tape&Reel
LP3401LT3G	A1	10000/Tape&Reel

4. MAXIMUM RATINGS($T_a = 25^\circ C$)

Parameter	Symbol	Limits	Unit
Drain–Source Voltage	V_{DS}	-30	V
Gate–to–Source Voltage – Continuous	V_{GS}	± 12	V
Drain Current			
– Continuous $T_A = 25^\circ C$ (Note 1)	I_D	-4.2	A
– Pulsed (Note 2)	I_{DM}	-16	
– Continuous(Note 3)	I_D	-2.4	A
– Pulsed (Note 3)	I_{DM}	-9.6	

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Power Dissipation(Note 1)	PD	1	W
Power Dissipation(Note 3)	PD	0.625	W
Thermal Resistance, Junction–to–Ambient(Note 1)	$R_{\theta JA}$	125	$^\circ C/W$
Junction–to–Ambient(Note 3)	$R_{\theta JA}$	200	
Junction–to–Case	$R_{\theta JC}$	100	
Junction and Storage temperature	T_J, T_{stg}	$-55 \sim +150$	$^\circ C$

Note 1.Surface mounted on "1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu.

2.Pulse width limited by maximum junction temperature.

3.Surface mounted on FR4 board using the minimum recommended pad size.

6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
STATIC						
Drain–Source Breakdown Voltage (VGS = 0 V, ID = -250 μA)		VBRDSS	-30	-	-	V
Gate-Source Threshold Voltage (VDS = VGS , ID = -250 μA)		VGS(th)	-0.6	-1.0	-1.3	V
Gate-Body Leakage Current (VDS = 0 V, VGS = ± 12 V)		IGSS	-	-	± 100	nA
Zero Gate Voltage Drain Current (VDS = -24 V, VGS = 0 V)		IDSS	-	-	-1	μA
Drain-Source On-Resistance(Note 4) (VGS = -10 V, ID = -4.2 A) (VGS = -4.5 V, ID = -4 A) (VGS = -2.5 V, ID = -1 A)		RDS(ON)	- - -	- - -	70 80 120	mΩ
DYNAMIC						
Total Gate Charge	(VDS = -15 V, VGS = -4.5 V,ID = -4 A)	Qg	-	7.4	-	nC
Gate-Source Charge		Qgs	-	1.3	-	
Gate-Drain Charge		Qgd	-	2.6	-	
Turn-On Delay Time	(VDS = -15 V, RL = 3.6 Ω, VGS= -10V, RGEN =6.2 Ω)	td(on)	-	2.6	-	ns
Rise Time		tr	-	10	-	
Turn-Off Delay Time		td(off)	-	52	-	
Fall Time		tf	-	16.2	-	
Input Capacitance	(VDS = -15 V, VGS = 0 V, f = 1 MHz)	Ciss	-	740	-	pF
Output Capacitance		Coss	-	51	-	
Reverse Transfer Capacitance		Crss	-	44	-	
Diode characteristics						
Diode Continuous Current TA = 25°C		IS	-	-	-1.1	A
Diode Plused Current TA = 25°C		ISM	-	-	-4.4	A
Diode Forward Voltage(Note 4) (IS = -1 A,VGS = 0 V)		VSD	-	-0.75	-1.3	V
Reverse Recovery Time (VR=-15V,IF=-2.1A,dIF/dt=85A/us)		trr	-	39	-	ns
Reverse Recovery Charge (VR=-15V,IF=-2.1A,dIF/dt=85A/us)		Qrr	-	9.6	-	nC
Reverse Recovery Current (VR=-15V,IF=-2.1A,dIF/dt=85A/us)		IRRM	-	-0.5	-	A

3. Pulse test: PW $\leq$ 300us duty cycle $\leq$ 2%.

7. ELECTRICAL CHARACTERISTICS CURVES

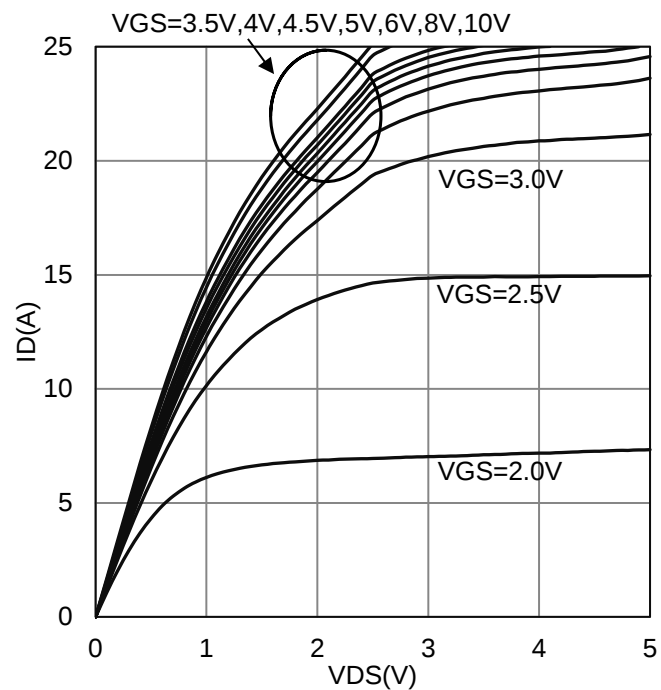


Figure 1.ID vs. VDS

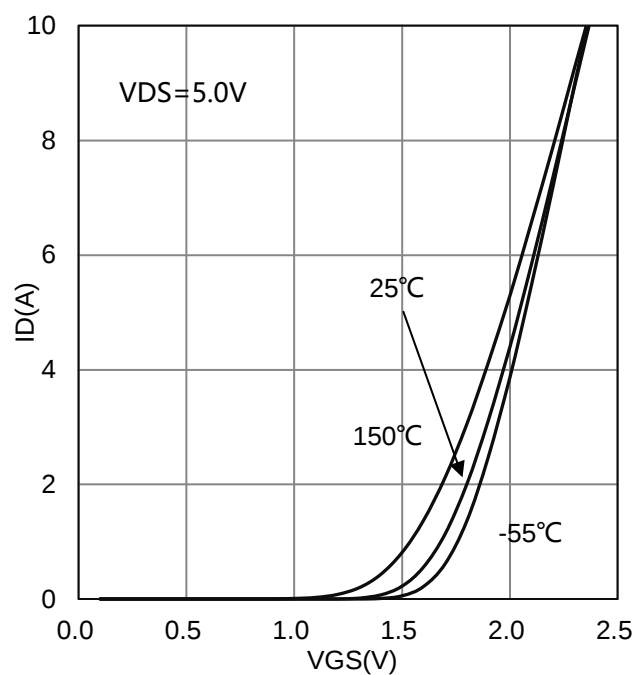


Figure 2.ID vs. VGS

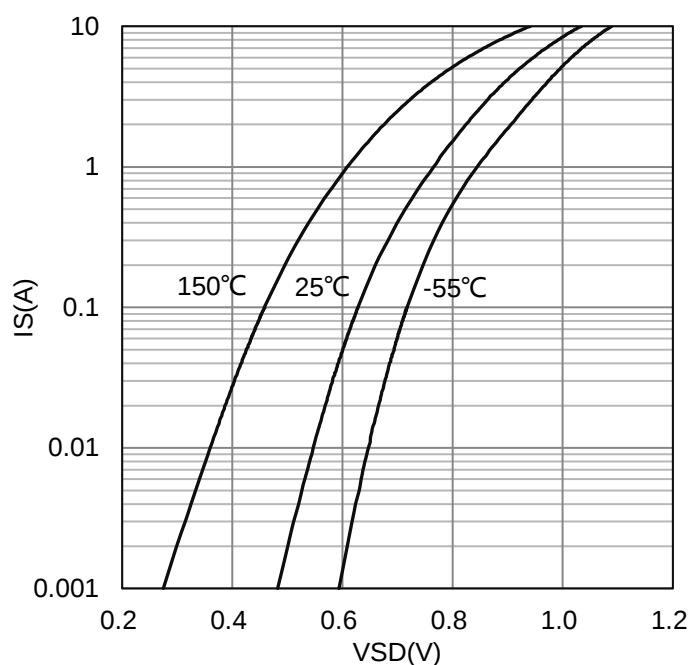


Figure 3.IS vs. VSD

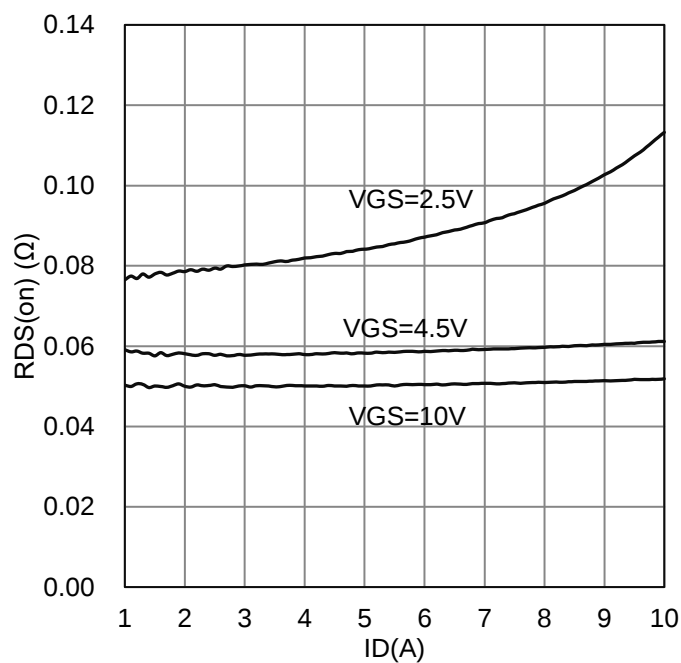


Figure 4.RDS(on) vs. ID

7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

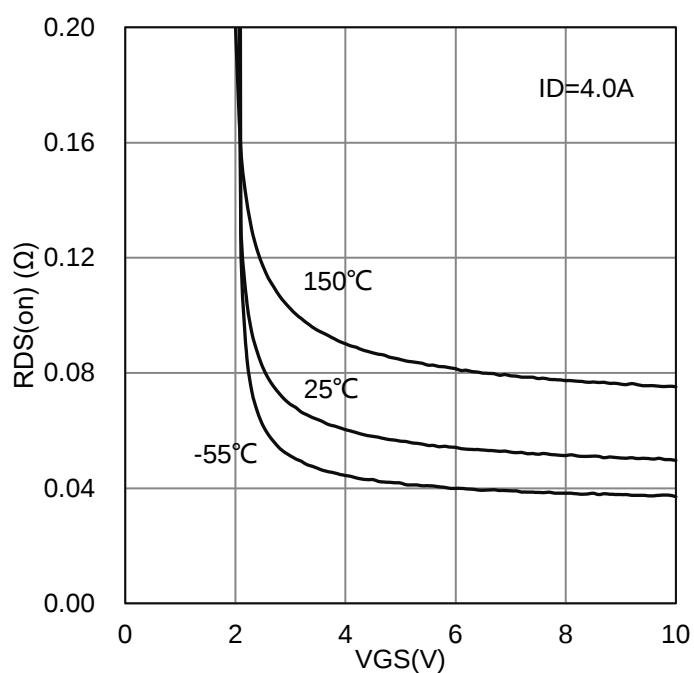


Figure 5. $R_{DS(on)}$ vs. V_{GS}

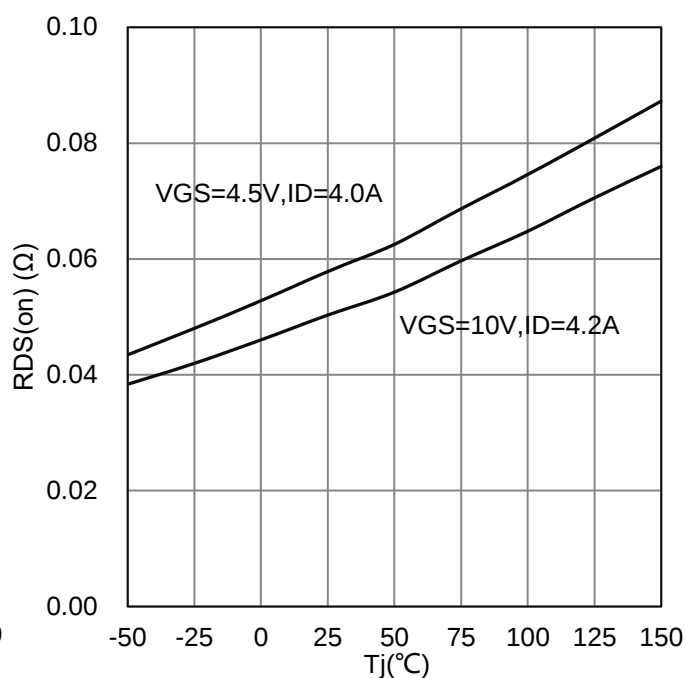


Figure 6. $R_{DS(on)}$ vs. T_j

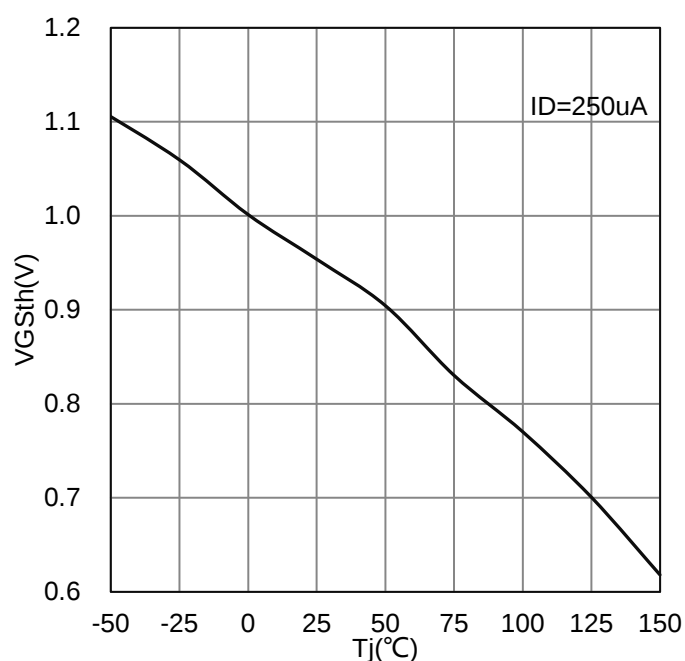


Figure 7. V_{GSth} vs. T_j

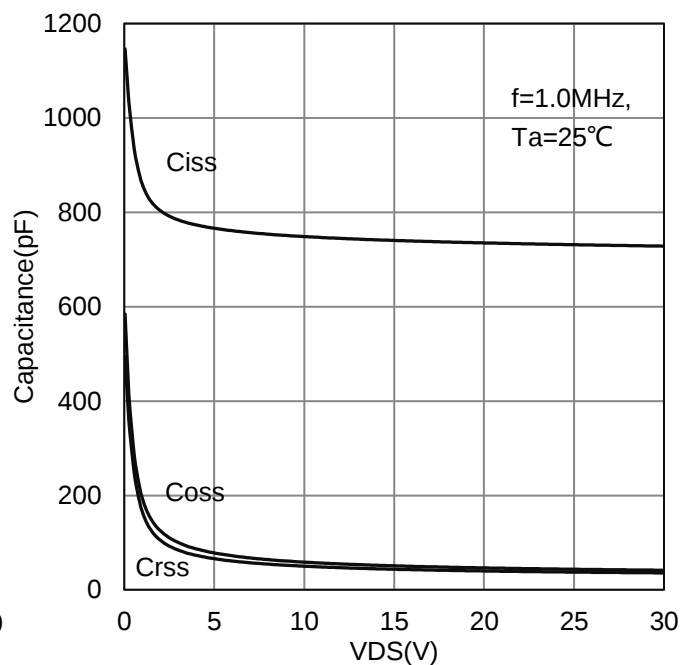


Figure 8. Capacitance

7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

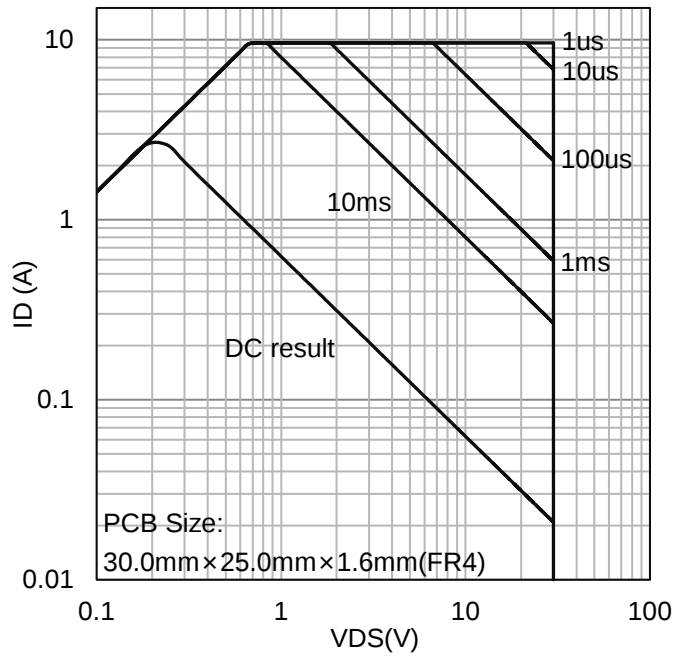


Figure 9.Safe Operating Area

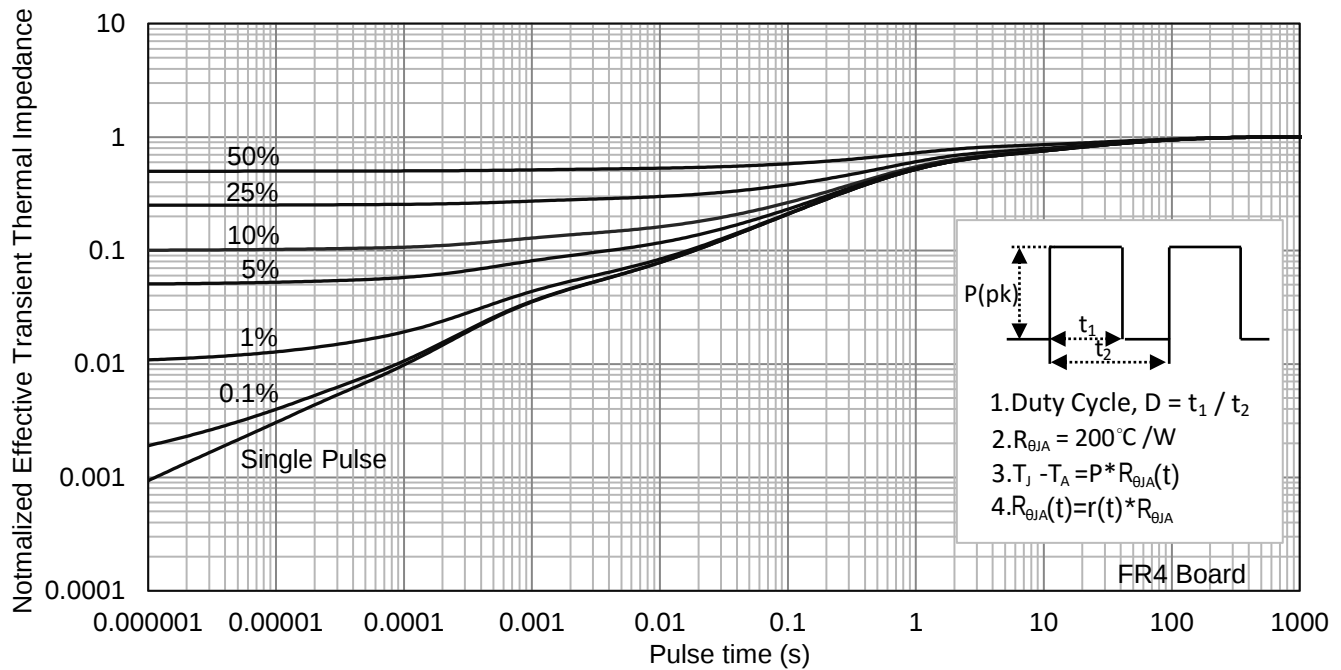
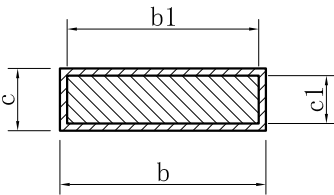
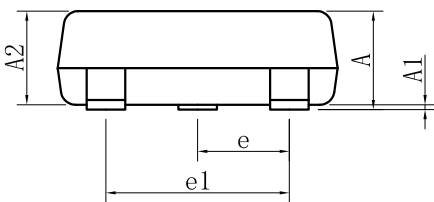
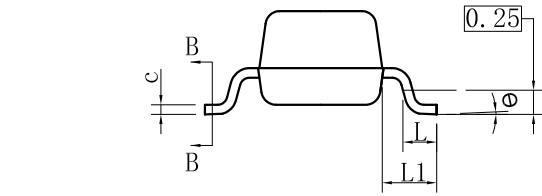
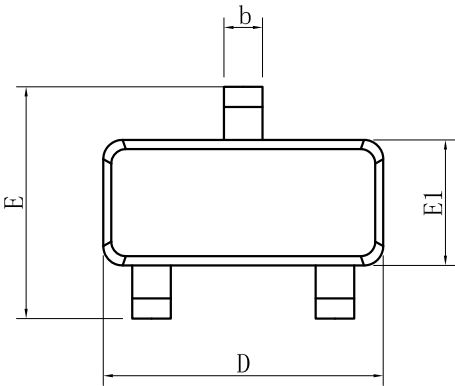


Figure 10.Thermal Response

8.OUTLINE AND DIMENSIONS



SECTION B-B

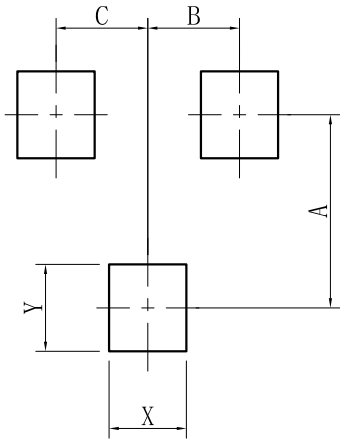


SOT23			
DIM	MIN	NOR	MAX
A	0.89	—	1.12
A1	0.01	—	0.10
A2	0.88	0.95	1.02
b	0.30	—	0.50
b1	0.30	0.40	0.45
c	0.08	—	0.20
c1	0.08	0.10	0.16
D	2.80	2.90	3.04
E	2.10	—	2.64
E1	1.20	1.30	1.40
e	0.95BSC		
e1	1.90BSC		
L	0.40	0.46	0.60
L1	0.54REF		
θ	0°	—	8°
All Dimensions in mm			

GENERAL NOTES

- 1.Top package surface finish Ra0.4±0.2um
- 2.Bottom package surface finish Ra0.7±0.2um
- 3.Side package surface finish Ra0.4±0.2um

9.SOLDERING FOOTPRINT



SOT23	
DIM	(mm)
X	0.80
Y	0.90
A	2.00
B	0.95
C	0.95

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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