

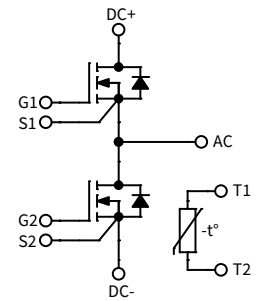
CAB7R5A23GM4, CAB7R5A23GM4T

2300 V, 7.5 mΩ, Silicon Carbide, Half-Bridge Module

V_{DS}	2300 V
$R_{DS(on)}$	7.5 mΩ

Technical Features

- Fully SiC MOSFET-based for Ultra-Low Loss
- Press-fit Pins for Easy Assembly
- Aluminium Nitride Substrate
- Optional Pre-Applied Thermal Interface Material
- Features Gen4 Technology with Soft Body Diode
- Conforms to UL STD 1557



Typical Applications

- High-Efficiency Converters / Inverters
- Energy Storage Systems
- Renewable Energy
- Smart-Grid / Grid-Tied Distributed Generation
- Solar Inverters
- DC Fast Chargers

System Benefits

- Enables Compact, Lightweight Systems
- Enables Two-Level Conversion for 1500 VDC Systems
- Increased System Efficiency due to Low Switching & Conduction Losses of SiC
- Reduced Thermal Requirements and System Cost

Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Voltage	V_{DS}			2300	V		
Maximum Gate-Source Voltage	$V_{GS(max)}$	-10		+23		Transient	Fig. 33
Operational Gate-Source Voltage	$V_{GS(op)}$		-4/+15..18			Static	Note 1
DC Continuous Drain Current	I_D			150	A	$V_{GS} = 15 \text{ V}, T_{HS} = 75^\circ\text{C}, T_{VJ} \leq 150^\circ\text{C}$	Notes 2,3,4 Fig. 20
DC Source-Drain Current (Body Diode)	$I_{SD BD}$		95			$V_{GS} = -4 \text{ V}, T_{HS} = 75^\circ\text{C}, T_{VJ} \leq 150^\circ\text{C}$	
Pulsed Drain Current	I_{DM}			600		t_{Pmax} limited by T_{VJmax} $V_{GS} = 15 \text{ V}, T_{HS} = 75^\circ\text{C}$	
Power Dissipation	P_D		510		W	$T_{HS} = 75^\circ\text{C}, T_{VJ} \leq 150^\circ\text{C}$	Note 5 Fig. 21
Virtual Junction Temperature	$T_{VJ(op)}$	-40		150	$^\circ\text{C}$	Operation	

Note (1): Recommended turn-on gate voltage is 15 V with $\pm 5\%$ regulation tolerance

Note (2): Current limit at $T_{HS} = 75^\circ\text{C}, T_{VJ} \leq 150^\circ\text{C}$ imposed by package

Note (3): Continuous DC operational limit set by DC- pins. See Figure 22 for implementable AC current

Note (4): Verified by design

Note (5): $P_D = (T_{VJ} - T_{HS})/R_{TH(JH,typ)}$

MOSFET Characteristics (Per Position) ($T_{vj} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	2300				$V_{GS} = 0\text{ V}$, $T_{vj} = -40\text{ }^{\circ}\text{C}$	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	4.0	V	$V_{DS} = V_{GS}$, $I_D = 76\text{ mA}$	
			2.1			$V_{DS} = V_{GS}$, $I_D = 76\text{ mA}$, $T_{vj} = 150\text{ }^{\circ}\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}		10	600	μA	$V_{GS} = 0\text{ V}$, $V_{DS} = 2300\text{ V}$	
Gate-Source Leakage Current	I_{GSS}		50	1000	nA	$V_{GS} = 15\text{ V}$, $V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		7.5	10.5	m Ω	$V_{GS} = 15\text{ V}$, $I_D = 160\text{ A}$	Fig. 2 Fig. 3
			18			$V_{GS} = 15\text{ V}$, $I_D = 160\text{ A}$, $T_{vj} = 150\text{ }^{\circ}\text{C}$	
			7			$V_{GS} = 18\text{ V}$, $I_D = 160\text{ A}$	
			17.6			$V_{GS} = 18\text{ V}$, $I_D = 160\text{ A}$, $T_{vj} = 150\text{ }^{\circ}\text{C}$	
Transconductance	g_{fs}		175		S	$V_{DS} = 20\text{ V}$, $I_D = 160\text{ A}$	Fig. 4
			170			$V_{DS} = 20\text{ V}$, $I_D = 160\text{ A}$, $T_{vj} = 150\text{ }^{\circ}\text{C}$	
Turn-On Switching Energy, $T_{vj} = 25\text{ }^{\circ}\text{C}$ $T_{vj} = 125\text{ }^{\circ}\text{C}$ $T_{vj} = 150\text{ }^{\circ}\text{C}$	E_{On}		3.1 3.2 3.2		mJ	$V_{DD} = 1200\text{ V}$, $I_D = 160\text{ A}$, $V_{GS} = -4\text{ V}/15\text{ V}$, $R_{G(OFF)} = 0.0\text{ }\Omega$, $R_{G(ON)} = 0.0\text{ }\Omega$, $L_G = 18\text{ nH}$	Fig. 11 Fig. 13
Turn-Off Switching Energy, $T_{vj} = 25\text{ }^{\circ}\text{C}$ $T_{vj} = 125\text{ }^{\circ}\text{C}$ $T_{vj} = 150\text{ }^{\circ}\text{C}$	E_{Off}		2.3 2.4 2.5				
Internal Gate Resistance	$R_{G(int)}$		1.6		Ω	$f = 100\text{ kHz}$	
Input Capacitance	C_{iss}		24.4		nF	$V_{GS} = 0\text{ V}$, $V_{DS} = 1500\text{ V}$, $V_{AC} = 25\text{ mV}$, $f = 100\text{ kHz}$	Fig. 9
Output Capacitance	C_{oss}		0.40				
Reverse Transfer Capacitance	C_{rss}		32		pF		
Gate to Source Charge	Q_{GS}		185		nC	$V_{DS} = 1500\text{ V}$, $V_{GS} = -4\text{ V}/15\text{ V}$, $I_D = 160\text{ A}$, Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		155				
Total Gate Charge	Q_G		590				
FET Thermal Resistance, Junction to Heatsink	$R_{th JHS}$		0.145		$^{\circ}\text{C}/\text{W}$	Measured with Pre-Applied TIM	Fig. 17

Diode Characteristics (Per Position) ($T_{VJ} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Notes
Body Diode Forward Voltage	V_{SD}		5.8		V	$V_{GS} = -4\text{ V}$, $I_{SD} = 160\text{ A}$	Fig. 7
			5.3			$V_{GS} = -4\text{ V}$, $I_{SD} = 160\text{ A}$, $T_{VJ} = 150\text{ }^{\circ}\text{C}$	
Reverse Recovery Time	t_{RR}		46		ns	$V_{GS} = -4\text{ V}$, $I_{SD} = 160\text{ A}$, $V_R = 1200\text{ V}$ $di/dt = 17\text{ A/ns}$, $T_{VJ} = 150\text{ }^{\circ}\text{C}$	Fig. 32
Reverse Recovery Charge	Q_{RR}		4.6		μC		
Peak Reverse Recovery Current	I_{RRM}		215		A		
Reverse Recovery Energy, $T_{VJ} = 25\text{ }^{\circ}\text{C}$ $T_{VJ} = 125\text{ }^{\circ}\text{C}$ $T_{VJ} = 150\text{ }^{\circ}\text{C}$	E_{RR}		1.4 2.6 3.9		mJ	$V_{DD} = 1200\text{ V}$, $I_D = 160\text{ A}$, $V_{GS} = -4\text{ V}/15\text{ V}$, $R_{G(ON)} = 0.0\text{ }\Omega$, $L_{\sigma} = 18\text{ nH}$	Fig. 14

Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Package Resistance, M1 (High-Side)	R_{pkg1}		1.5		m Ω	$T_C = 125\text{ }^{\circ}\text{C}$, Note 6
Package Resistance, M2 (Low-Side)	R_{pkg2}		1.4			
Stray Inductance	L_{Stray}		11		nH	Between DC- and DC+, $f = 10\text{ MHz}$
Case Temperature	T_C	-40		125	$^{\circ}\text{C}$	
Mounting Torque	M_S		2.0	2.3	N-m	M4 bolts
Weight	W		36		g	
Case Isolation Voltage	V_{isol}	5			kV	AC, 50 Hz, 1 minute
Comparative Tracking Index	CTI	600				
Clearance Distance			8.1		mm	Terminal to Terminal
			13.2			Terminal to Heatsink
Creepage Distance			9.8			Terminal to Terminal
			14.9			Terminal to Heatsink

Note (6): Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance

Temperature Sensor (NTC) Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rated Resistance	R_{NTC}		5.0		k Ω	$T_{NTC} = 25\text{ }^{\circ}\text{C}$
Resistance Tolerance at $25\text{ }^{\circ}\text{C}$	$\Delta R/R$	-5		5	%	
Beta Value ($T_2 = 50\text{ }^{\circ}\text{C}$)	$\beta_{25/50}$		3380		K	
Beta Value ($T_2 = 80\text{ }^{\circ}\text{C}$)	$\beta_{25/80}$		3468		K	
Beta Value ($T_2 = 100\text{ }^{\circ}\text{C}$)	$\beta_{25/100}$		3523		K	
Power Dissipation	P_{Max}			10	mW	$T_{NTC} = 25\text{ }^{\circ}\text{C}$

Typical Performance

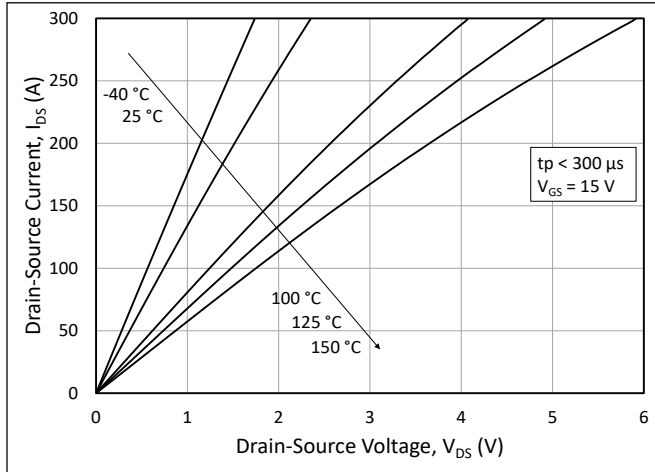


Figure 1. Output Characteristics for Various Junction Temperatures

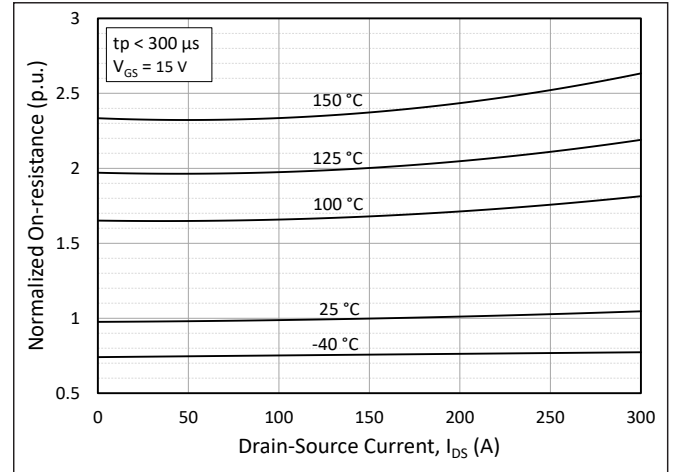


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

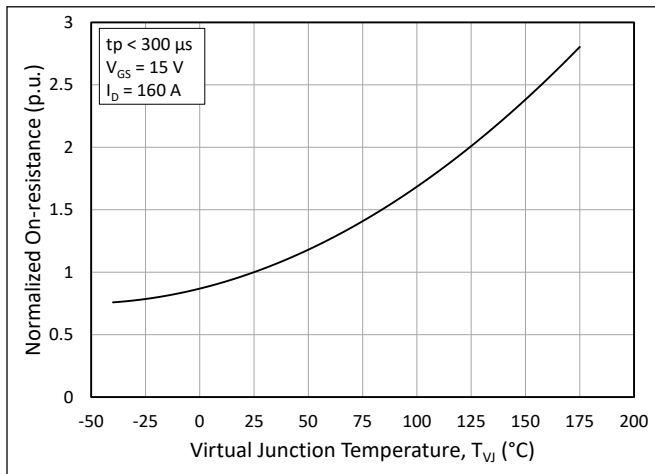


Figure 3. Normalized On-State Resistance vs. Junction Temperature

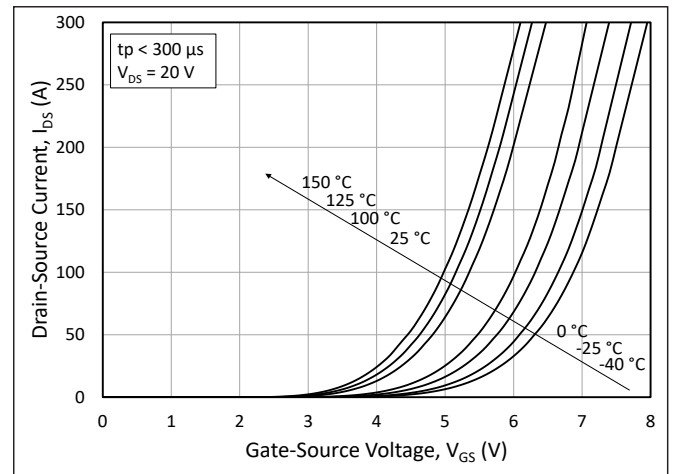


Figure 4. Transfer Characteristic for Various Junction Temperatures

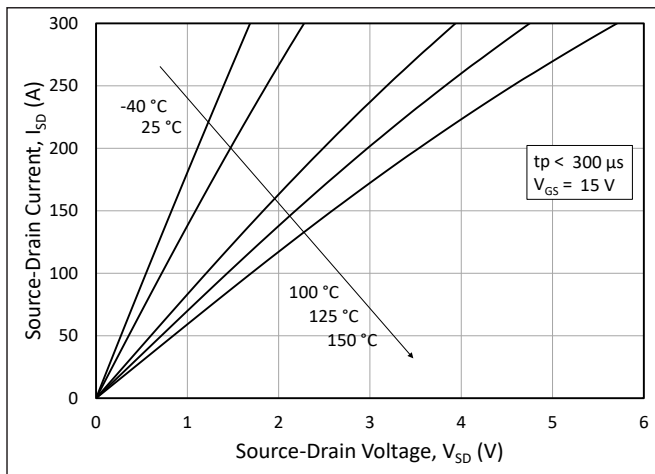


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 15 V$

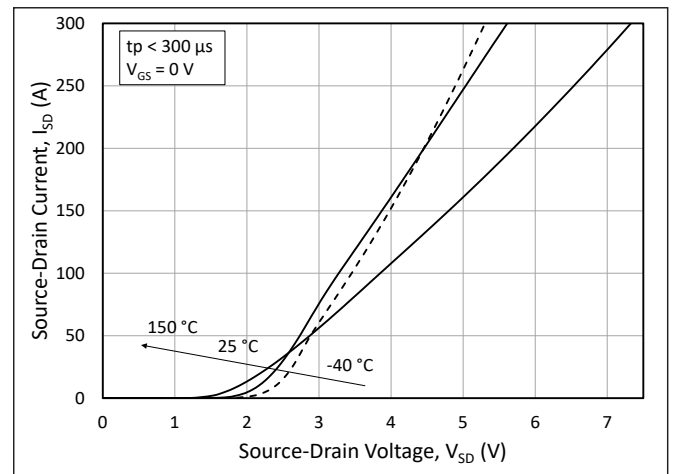


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 0 V$ (Body Diode)

Typical Performance

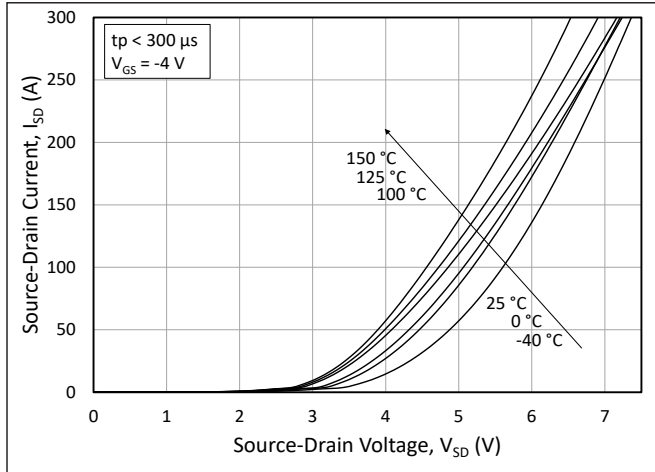


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = -4$ V (Body Diode)

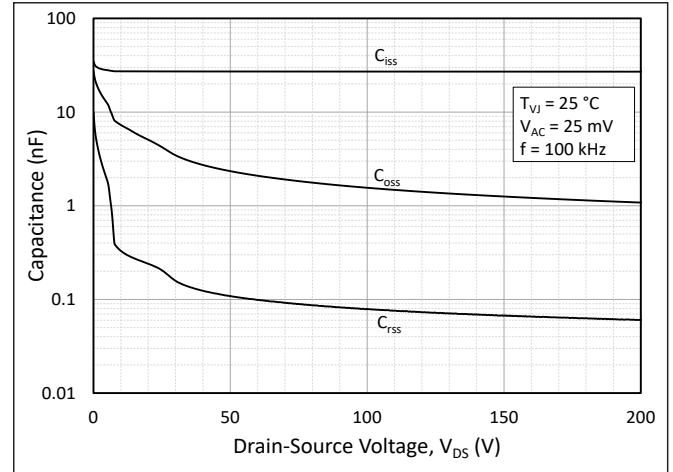


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200 V)

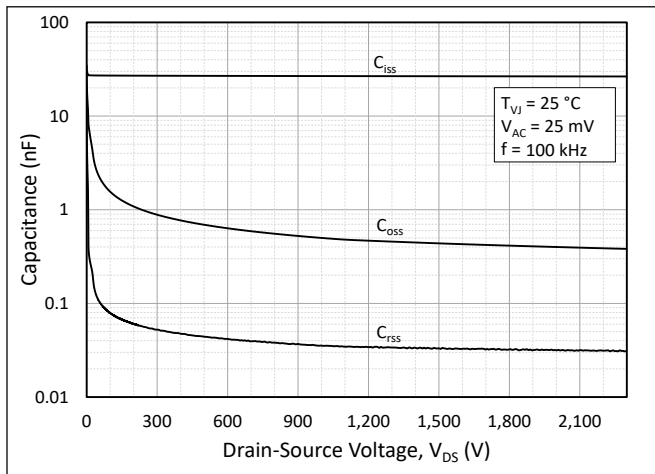


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 2300 V)

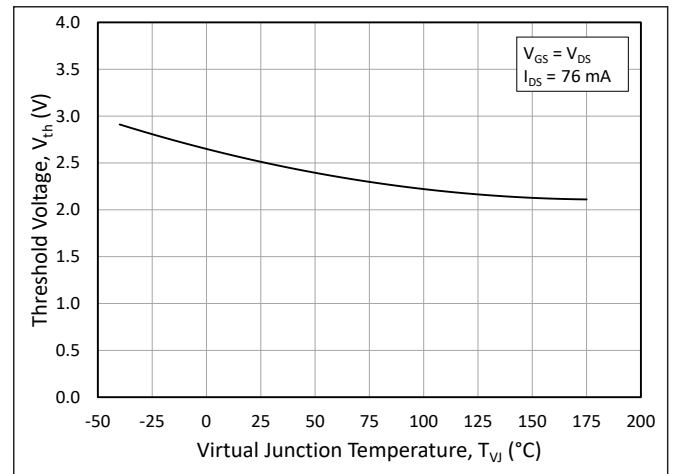


Figure 10. Threshold Voltage vs. Junction Temperature

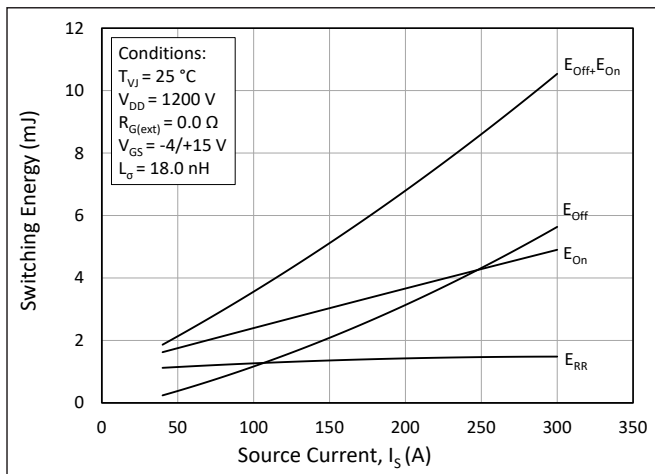


Figure 11. Switching Energy vs. Drain Current ($V_{DD} = 1200$ V)

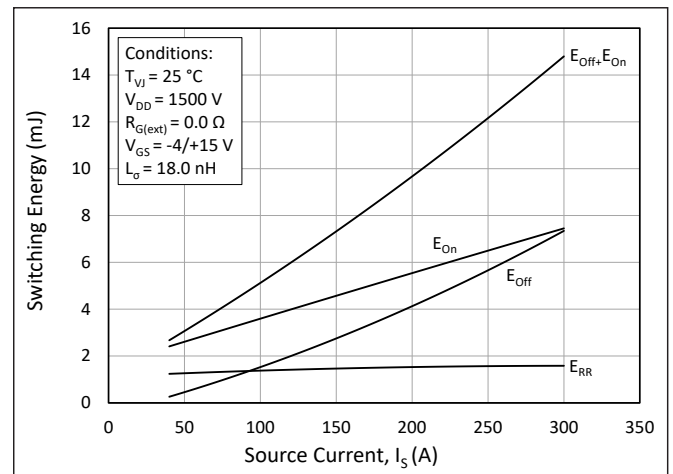


Figure 12. Switching Energy vs. Drain Current ($V_{DD} = 1500$ V)



Typical Performance

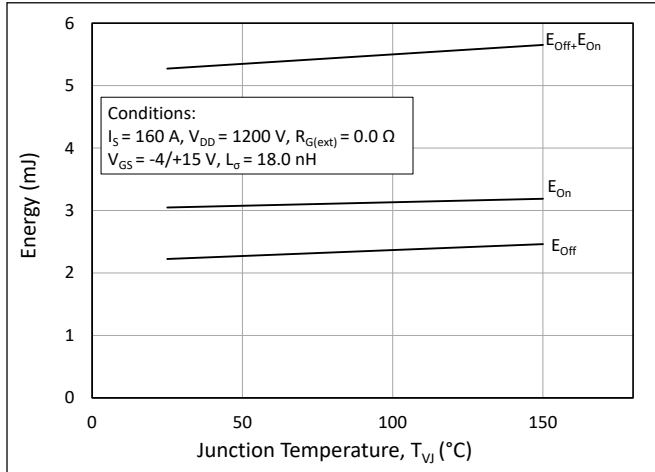


Figure 13. MOSFET Switching Energy vs. Junction Temperature

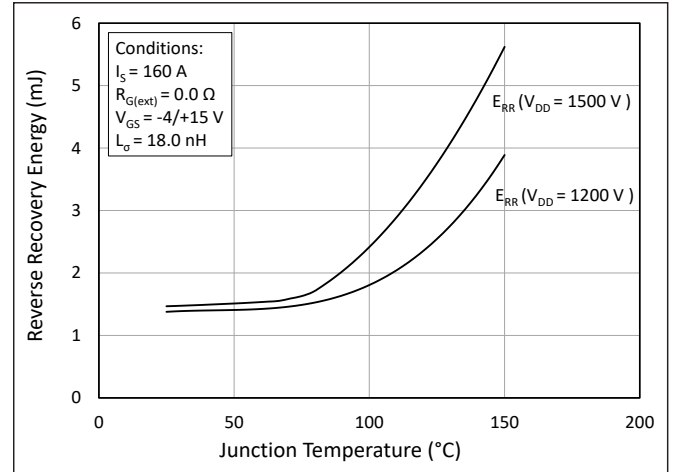


Figure 14. Reverse Recovery Energy vs. Junction Temperature

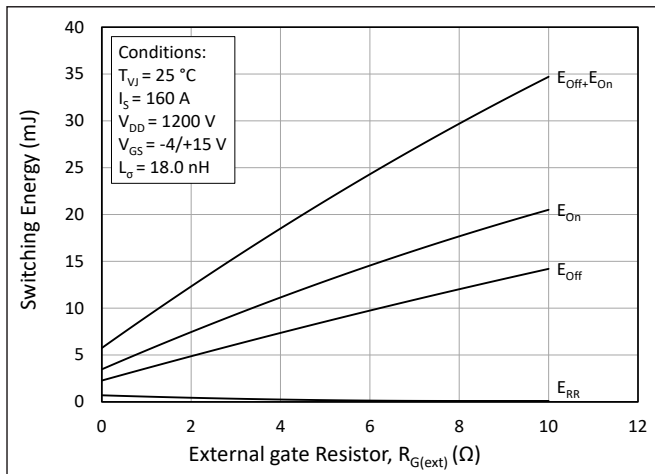


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

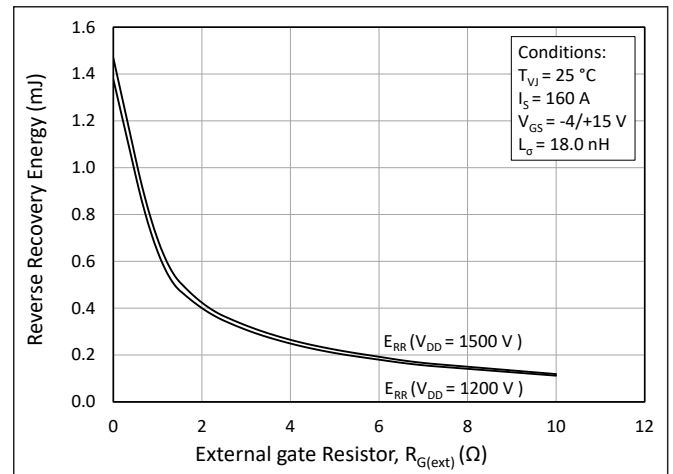


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

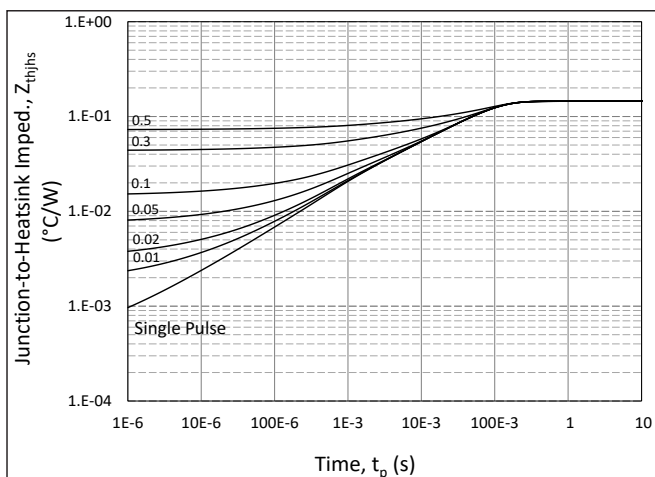


Figure 17. MOSFET Junction to Heatsink Transient Thermal Impedance, $Z_{\text{th JHS}}$ ($^{\circ}\text{C/W}$)

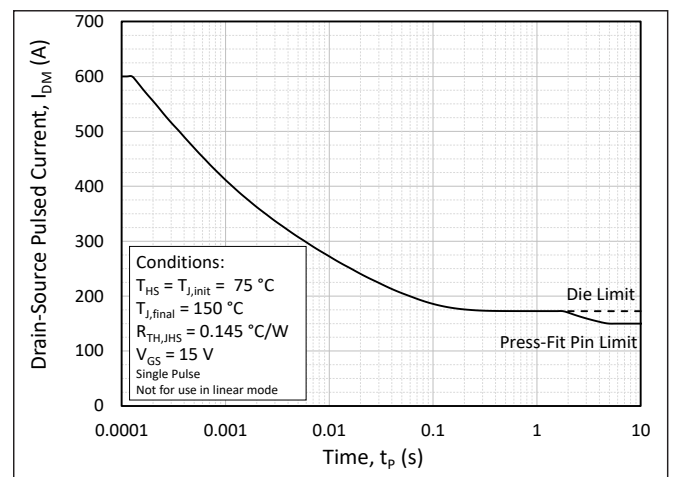
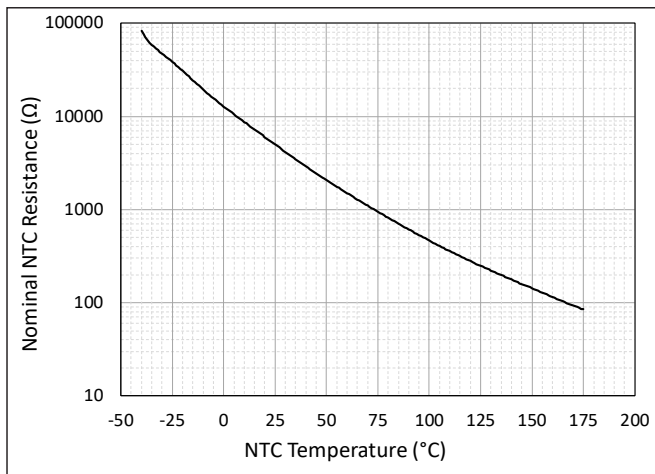
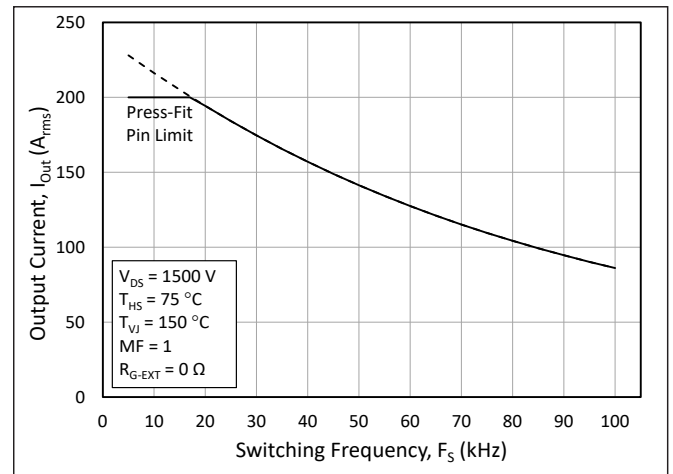
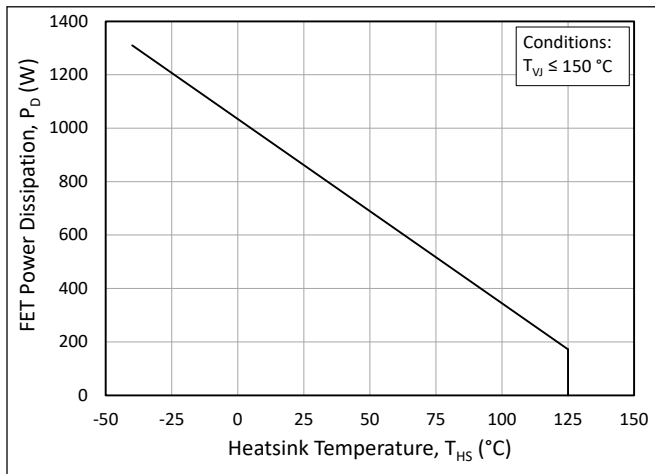
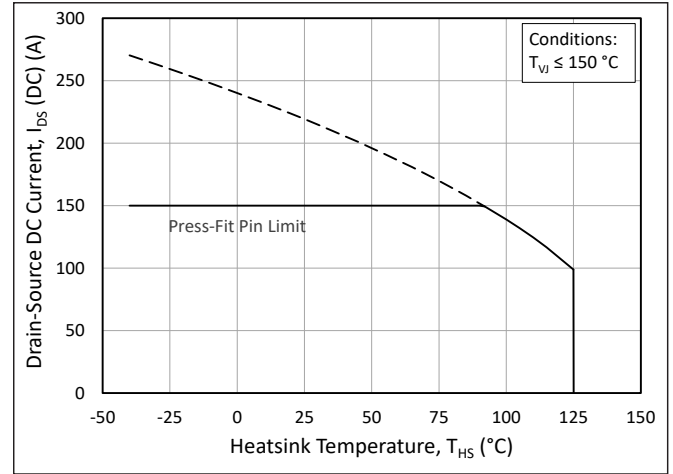
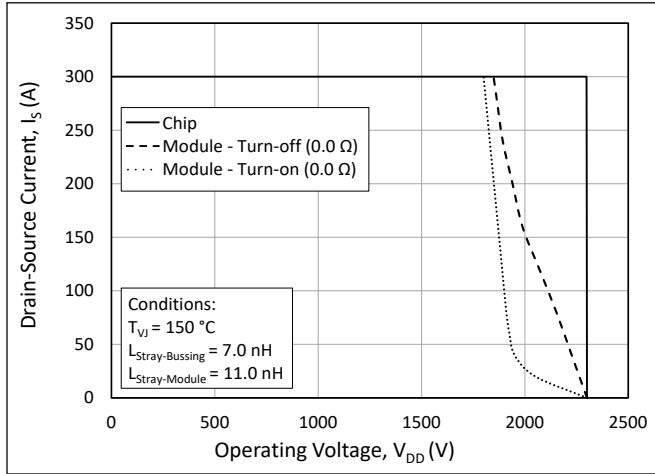


Figure 18. Pulsed Current Safe Operating Area (PCSOA)

Typical Performance



Timing Characteristics

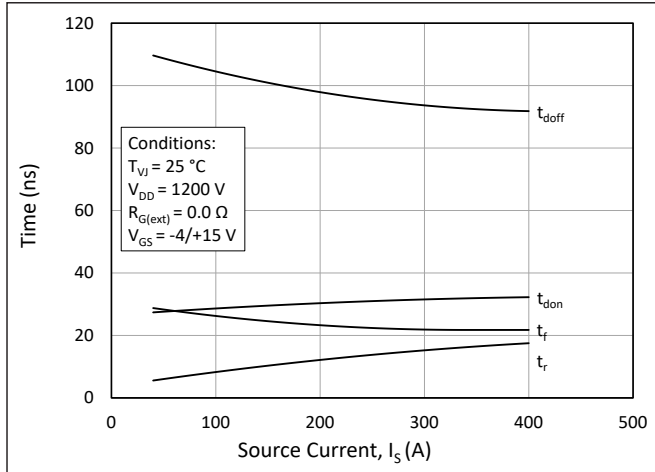


Figure 24. Timing vs. Source Current

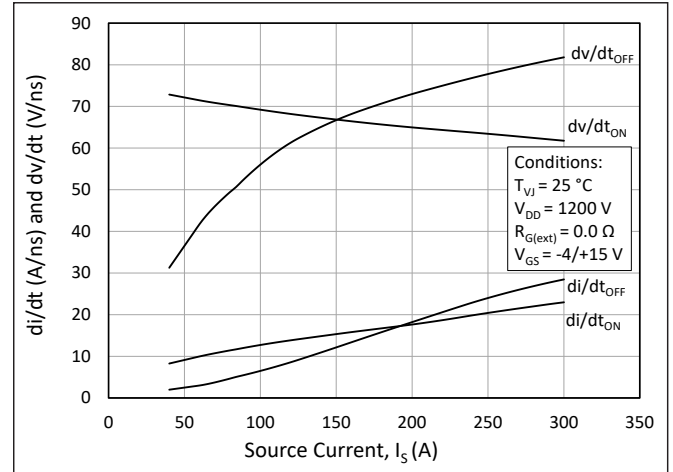


Figure 25. dv/dt and di/dt vs. Source Current

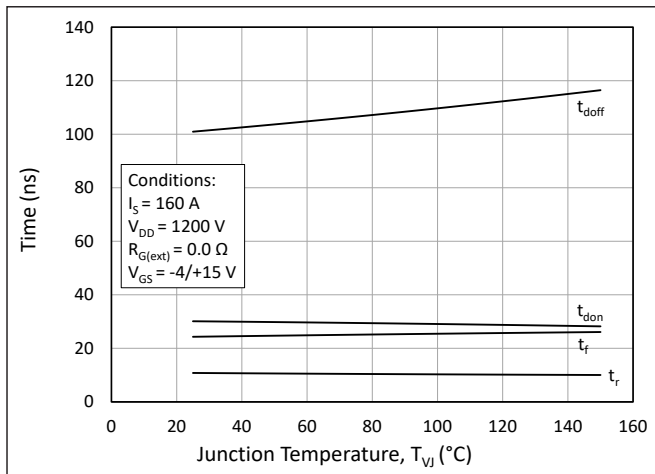


Figure 26. Timing vs. Junction Temperature

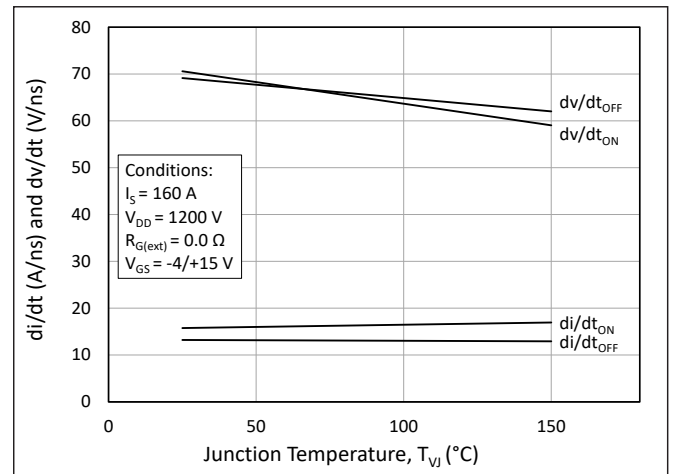


Figure 27. dv/dt and di/dt vs. Junction Temperature

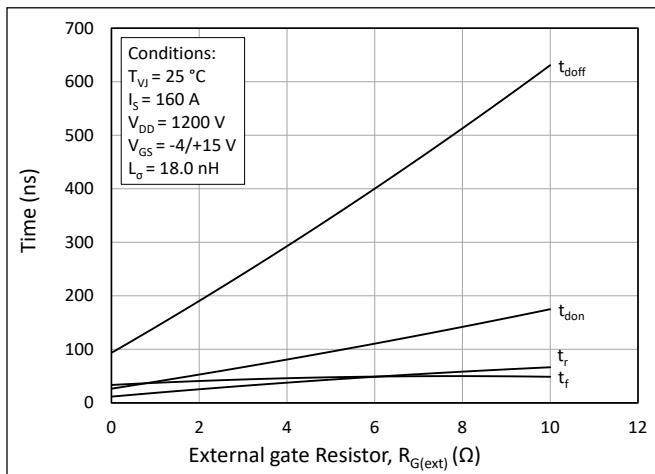


Figure 28. Timing vs. External Gate Resistance

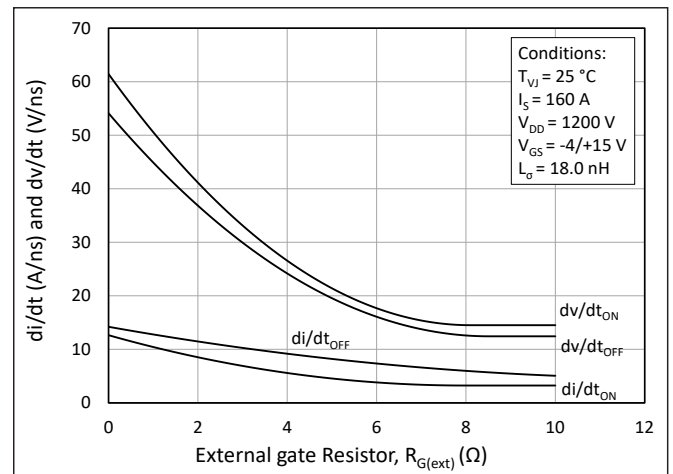


Figure 29. dv/dt and di/dt vs. External Gate Resistance

Definitions

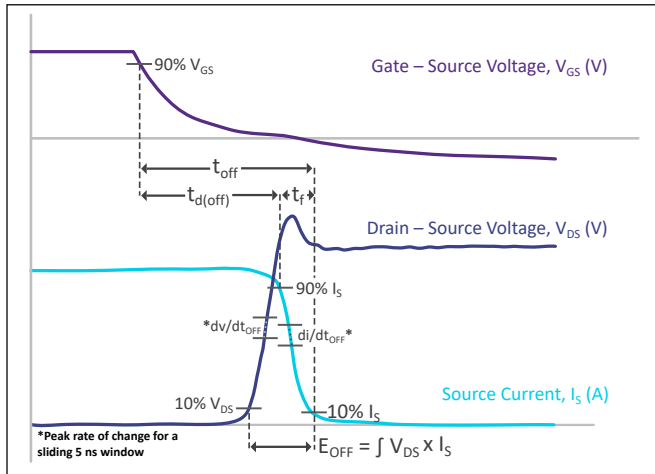


Figure 30. Turn-off Transient Definitions

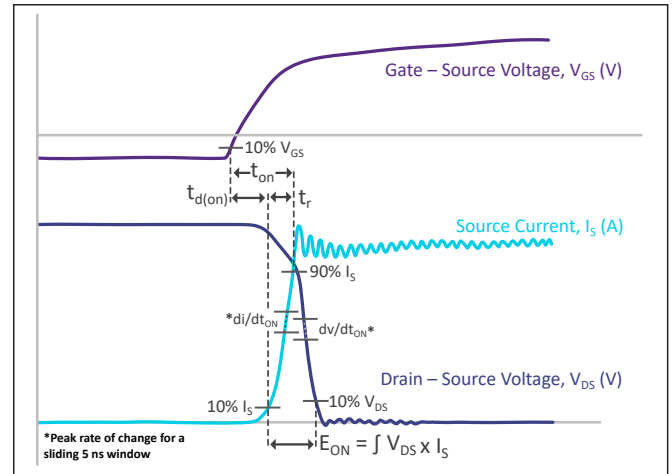


Figure 31. Turn-on Transient Definitions

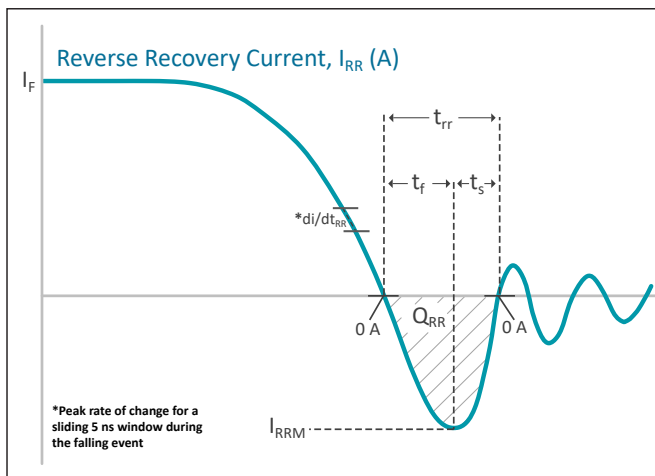


Figure 32. Reverse Recovery Definitions

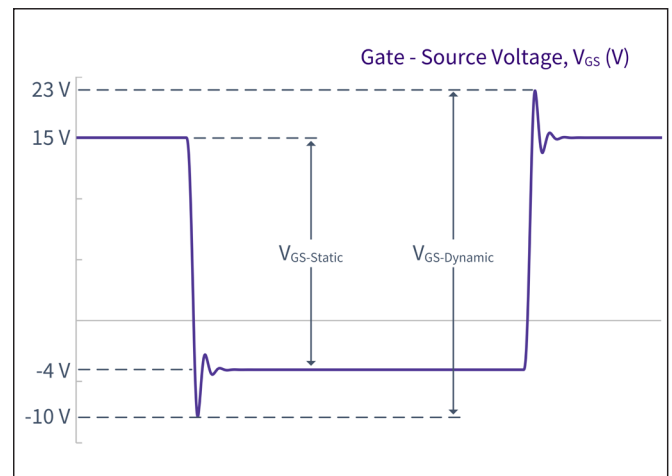
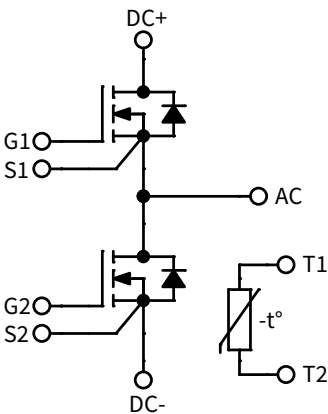
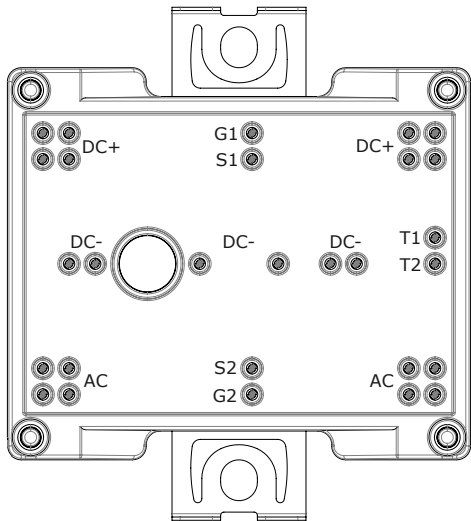


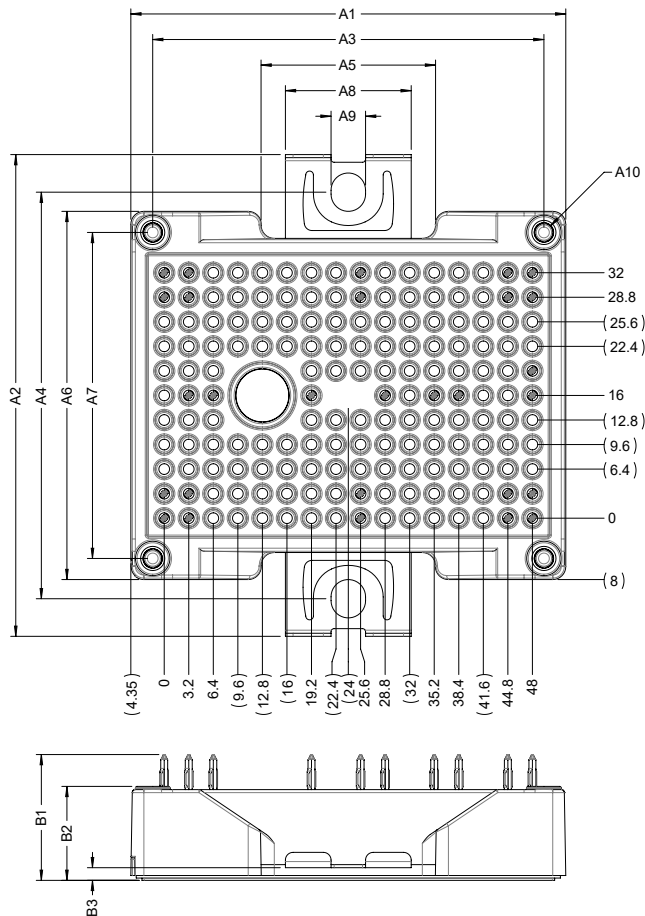
Figure 33. V_{GS} Transient Definitions

Note (7): A gate driver featuring the IXDD614SI gate driver IC was used to evaluate dynamic performance. The typical driver high-state output resistance of 0.4Ω and low-state output resistance of 0.3Ω are not included in the RG(ext) values on this datasheet.

Schematic and Pin Out



Package Dimension (mm)



DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	56.7	±0.30
A2	62.8	±0.50
A3	51	±0.15
A4	(53)	REF.
A5	22.7	±0.30
A6	48	±0.30
A7	42.5	±0.15
A8	16.4	±0.20
A9	4.5	±0.10
A10	∅2.3 ∇8.5	$\begin{matrix} \phi: +0 \\ -0.10 \\ \nabla: \pm0.30 \end{matrix}$
B1	16.4	±0.50
B2	12.25	±0.35
B3	1.65	±0.20
ALL PIN LOCATIONS		±0.40

Note (8): CAB7R5A23GM4 and CAB7R5AA23GM4T have been certified by Intertek Testing Solutions® as an “Electrically Isolated Semiconductor Devices – Component” in accordance with UL 1557. Only power modules that bear the ETL marking should be considered as being covered under the ETL Component Recognition Program.

Note (9): To improve product traceability, Wolfspeed products include Data Matrix Content barcodes in the form of ZZZZZZZZZZZZ-DDDDDD-XXXX-NN-NNNNNNNN, where -Z, -D, -X/-N represent product number, date code, and module serial number, respectively. For instance, CCB021M-12FM3T-IA2434-0018-0010468112 is a CCB021M12FM3T produced in 2024 week 34 with a unique serial number.



Product Ordering Code

Part Number	Description
CAB7R5A23GM4	Without Pre-Applied Phase Change Thermal Interface Material
CAB7R5A23GM4T	With Pre-Applied Phase Change Thermal Interface Material

Supporting Links & Tools

Evaluation Tools & Support

- [All LTSpice Models](#)
- [All PLECS Models](#)
- [SpeedFit® Design Simulator](#)
- [Technical Support Forum](#)

Dual-Channel Gate Driver Board

- [EVAL-ADUM4146WHB1Z: Analog Devices® Gate Driver Board](#)
- [UCC21710QDWEVM-054: Texas Instruments® Gate Driver Board](#)
- [Si823H-AxWA-KIT: Skyworks® Gate Driver Board](#)
- [ACPL-355JC: Broadcom® Gate Driver Board](#)
- [CGD1700HB2M-UNA: Wolfspeed Gate Driver Board](#)
- [CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers](#)

Application Notes

- [PRD-02302: WolfPACK™ Mounting Instructions and PCB Requirements](#)
- [PRD-04814: Design Options for Wolfspeed® Silicon Carbide MOSFET Gate Bias Power Supplies](#)
- [PRD-06379: Environmental Considerations for Power Electronics Systems](#)
- [PRD-07845: Power Module Baseplate Capacitance and Electromagnetic Compatibility](#)
- [PRD-07933: Wolfspeed Power Module Thermal Interface Material Application User Guide](#)
- [PRD-07968: Wolfspeed WolfPACK™ Dynamic Performance](#)
- [PRD-08333: Wolfspeed Module CIL Evaluation Kits User Guide](#)
- [PRD-08376: Thermal Characterization Methods and Applications](#)
- [PRD-08710: Measuring Stray Inductance in Power Electronics Systems](#)
- [PRD-08911: Considerations for Current Balancing in Paralleled SiC Power Modules](#)
- [PRD-09035: Power Module RC Thermal Models User Guide](#)



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