

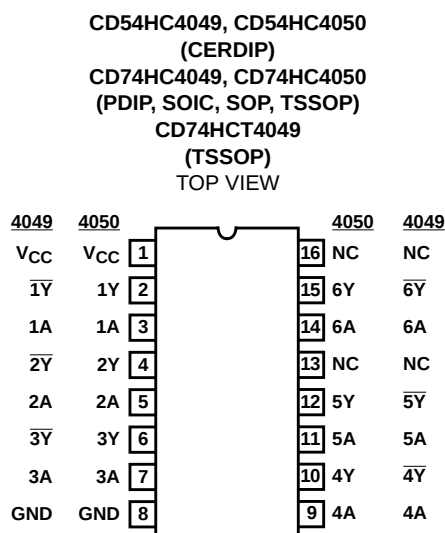
February 1998 - Revised November 2003

## High-Speed CMOS Logic Hex Buffers, Inverting and Non-Inverting

### Features

- Typical Propagation Delay: 6ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$
- High-to-Low Voltage Level Converter for up to  $V_I = 16V$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ C$  to  $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$

### Pinout



### Description

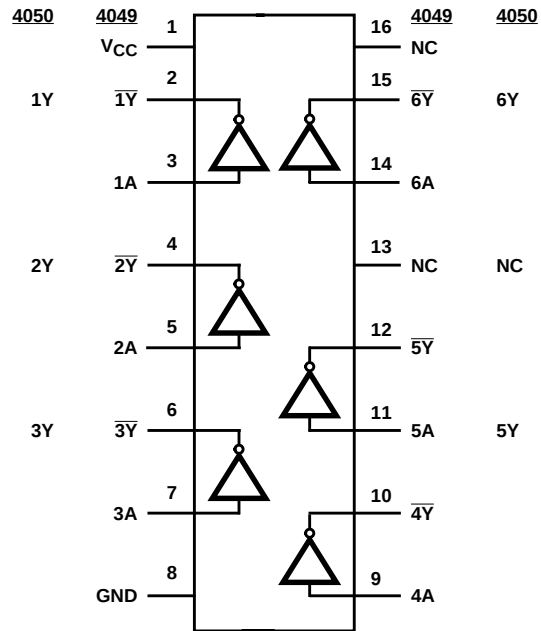
The 'HC4049 and 'HC4050 are fabricated with high-speed silicon gate technology. They have a modified input protection structure that enables these parts to be used as logic level translators which convert high-level logic to a low-level logic while operating off the low-level logic supply. For example, 15-V input pulse levels can be down-converted to 0-V to 5-V logic levels. The modified input protection structure protects the input from negative electrostatic discharge. These parts also can be used as simple buffers or inverters without level translation. The 'HC4049 and 'HC4050 are enhanced versions of equivalent CMOS types.

### Ordering Information

| PART NUMBER    | TEMP. RANGE<br>(°C) | PACKAGE      |
|----------------|---------------------|--------------|
| CD54HC4049F3A  | -55 to 125          | 16 Ld CERDIP |
| CD54HC4050F3A  | -55 to 125          | 16 Ld CERDIP |
| CD74HC4049E    | -55 to 125          | 16 Ld PDIP   |
| CD74HC4049M    | -55 to 125          | 16 Ld SOIC   |
| CD74HC4049MT   | -55 to 125          | 16 Ld SOIC   |
| CD74HC4049M96  | -55 to 125          | 16 Ld SOIC   |
| CD74HC4049NSR  | -55 to 125          | 16 Ld SOP    |
| CD74HC4049PW   | -55 to 125          | 16 Ld TSSOP  |
| CD74HC4049PWR  | -55 to 125          | 16 Ld TSSOP  |
| CD74HC4050E    | -55 to 125          | 16 Ld PDIP   |
| CD74HC4050M    | -55 to 125          | 16 Ld SOIC   |
| CD74HC4050MT   | -55 to 125          | 16 Ld SOIC   |
| CD74HC4050M96  | -55 to 125          | 16 Ld SOIC   |
| CD74HC4050NSR  | -55 to 125          | 16 Ld SOP    |
| CD74HC4050PW   | -55 to 125          | 16 Ld TSSOP  |
| CD74HC4050PWT  | -55 to 125          | 16 Ld TSSOP  |
| CD74HC4050PWR  | -55 to 125          | 16 Ld TSSOP  |
| CD74HCT4049PWT | -55 to 125          | 16 Ld TSSOP  |

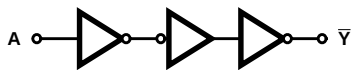
NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

## Functional Diagram

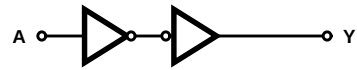


## Logic Diagrams

HC4049



HC4050



# CD54HC4049, CD74HC4049, CD54HC4050, CD74HC4050

## Absolute Maximum Ratings

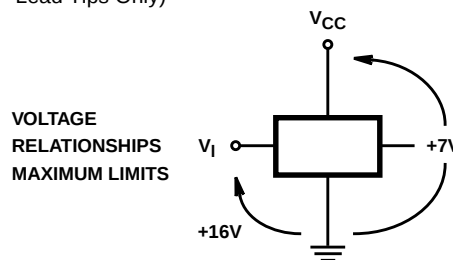
DC Supply Voltage,  $V_{CC}$  ..... -0.5V to 7V  
 DC Input Diode Current,  $I_{IK}$   
 For  $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Diode Current,  $I_{OK}$   
 For  $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Source or Sink Current per Output Pin,  $I_O$   
 For  $V_O > -0.5V$  or  $V_O < V_{CC} + 0.5V$  .....  $\pm 25mA$   
 DC  $V_{CC}$  or Ground Current,  $I_{CC}$  or  $I_{GND}$  .....  $\pm 50mA$

## Operating Conditions

Temperature Range ( $T_A$ ) ..... -55°C to 125°C  
 Supply Voltage Range,  $V_{CC}$   
 HC Types ..... 2V to 6V  
 HCT Types ..... 4.5V to 5.5V  
 DC Input or Output Voltage,  $V_I$ ,  $V_O$  ..... 0V to  $V_{CC}$   
 Input Rise and Fall Time  
 2V ..... 1000ns (Max)  
 4.5V ..... 500ns (Max)  
 6V ..... 400ns (Max)

## Thermal Information

Package Thermal Impedance,  $\theta_{JA}$  (see Note 1):  
 E (PDIP) Package ..... 67°C/W  
 M (SOIC) Package ..... 73°C/W  
 NS (SOP) Package ..... 64°C/W  
 PW (TSSOP) Package ..... 108°C/W  
 Maximum Junction Temperature (Hermetic Package or Die) ... 175°C  
 Maximum Junction Temperature (Plastic Package) ..... 150°C  
 Maximum Storage Temperature Range ..... -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) ..... 300°C  
 (SOIC - Lead Tips Only)



**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL          | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V) | 25°C |     |      | −40°C TO 85°C |      | −55°C TO 125°C |      | UNITS |
|-----------------------------------------|-----------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|------|-------|
|                                         |                 | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX  |       |
| HC TYPES                                |                 |                                    |                     |                     |      |     |      |               |      |                |      |       |
| High Level Input Voltage                | V <sub>IH</sub> | -                                  | -                   | 2                   | 1.5  | -   | -    | 1.5           | -    | 1.5            | -    | V     |
|                                         |                 |                                    |                     | 4.5                 | 3.15 | -   | -    | 3.15          | -    | 3.15           | -    | V     |
|                                         |                 |                                    |                     | 6                   | 4.2  | -   | -    | 4.2           | -    | 4.2            | -    | V     |
| Low Level Input Voltage                 | V <sub>IL</sub> | -                                  | -                   | 2                   | -    | -   | 0.5  | -             | 0.5  | -              | 0.5  | V     |
|                                         |                 |                                    |                     | 4.5                 | -    | -   | 1.35 | -             | 1.35 | -              | 1.35 | V     |
|                                         |                 |                                    |                     | 6                   | -    | -   | 1.8  | -             | 1.8  | -              | 1.8  | V     |
| High Level Output Voltage<br>CMOS Loads | V <sub>OH</sub> | V <sub>IH</sub> or V <sub>IL</sub> | −0.02               | 2                   | 1.9  | -   | -    | 1.9           | -    | 1.9            | -    | V     |
|                                         |                 |                                    | −0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -    | V     |
|                                         |                 |                                    | −0.02               | 6                   | 5.9  | -   | -    | 5.9           | -    | 5.9            | -    | V     |
| High Level Output Voltage<br>TTL Loads  | V <sub>OH</sub> | V <sub>IH</sub> or V <sub>IL</sub> | −4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -    | V     |
|                                         |                 |                                    | −5.2                | 6                   | 5.48 | -   | -    | 5.34          | -    | 5.2            | -    | V     |
| Low Level Output Voltage<br>CMOS Loads  | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 2                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 6                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| Low Level Output Voltage<br>TTL Loads   | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
|                                         |                 |                                    | 5.2                 | 6                   | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
| Input Leakage Current                   | I <sub>I</sub>  | V <sub>CC</sub> or GND             | -                   | 6                   | -    | -   | ±0.1 | -             | ±1   | -              | ±1   | μA    |
|                                         |                 | 15                                 | -                   | 6                   | -    | -   | ±0.5 | -             | ±5   | -              | ±5   |       |
| Quiescent Device Current                | I <sub>CC</sub> | V <sub>CC</sub> or GND             | 0                   | 6                   | -    | -   | 2    | -             | 20   | -              | 40   | μA    |

# CD54HC4049, CD74HC4049, CD54HC4050, CD74HC4050

## Switching Specifications Input $t_r, t_f = 6\text{ns}$

| PARAMETER                                                | SYMBOL                              | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|----------------------------------------------------------|-------------------------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                                          |                                     |                       |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| HC TYPES                                                 |                                     |                       |                     |      |     |     |               |     |                |     |       |
| Propagation Delay,<br>nA to nY HC4049<br>nA to nY HC4050 | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 85  | -             | 105 | -              | 130 | ns    |
|                                                          |                                     |                       | 4.5                 | -    | -   | 17  | -             | 21  | -              | 26  | ns    |
|                                                          |                                     |                       | 6                   | -    | -   | 14  | -             | 18  | -              | 22  | ns    |
|                                                          |                                     | C <sub>L</sub> = 15pF | 5                   | -    | 6   | -   | -             | -   | -              | -   | ns    |
| Transition Times (Figure 1)                              | t <sub>TLH</sub> , t <sub>THL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 75  | -             | 95  | -              | 110 | ns    |
|                                                          |                                     |                       | 4.5                 | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
|                                                          |                                     |                       | 6                   | -    | -   | 13  | -             | 16  | -              | 19  | ns    |
| Input Capacitance                                        | C <sub>I</sub>                      | -                     | -                   | -    | -   | 10  | -             | 10  | -              | 10  | pF    |
| Power Dissipation Capacitance<br>(Notes 2, 3)            | C <sub>PD</sub>                     | -                     | 5                   | -    | 35  | -   | -             | -   | -              | -   | pF    |

### NOTES:

- $C_{PD}$  is used to determine the dynamic power consumption, per gate.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

## Test Circuit and Waveform

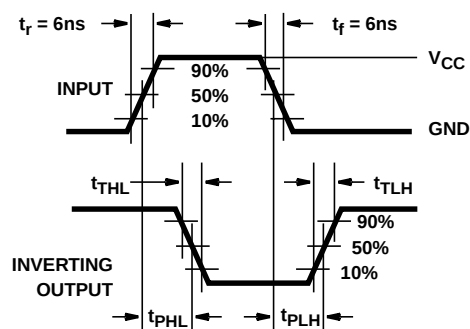
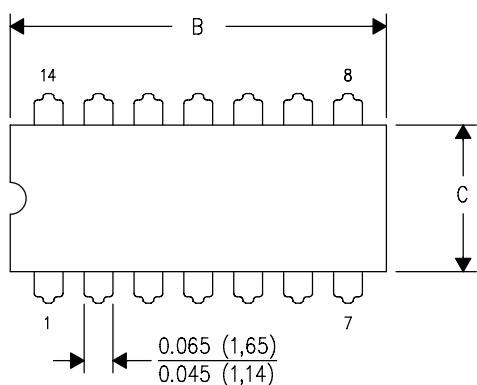


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

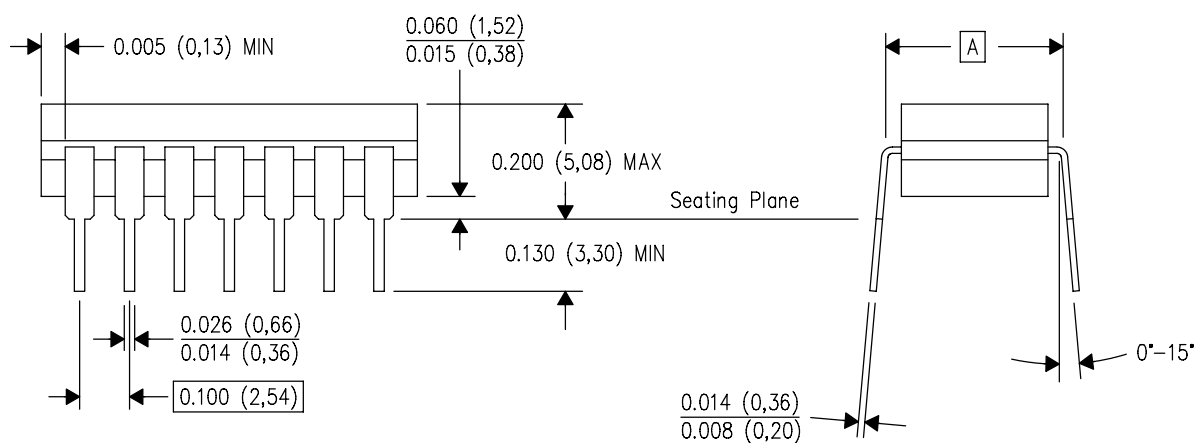
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



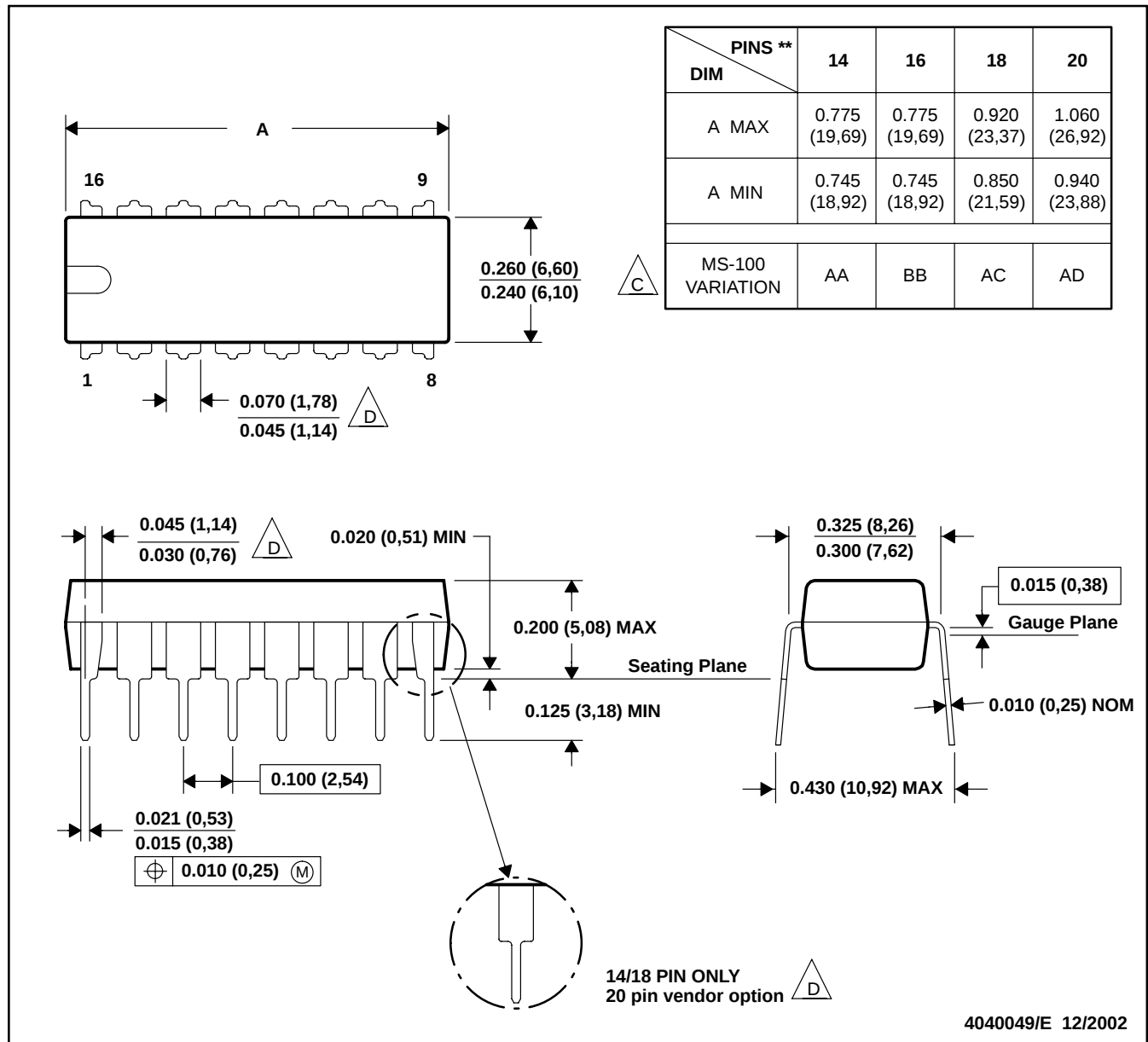
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

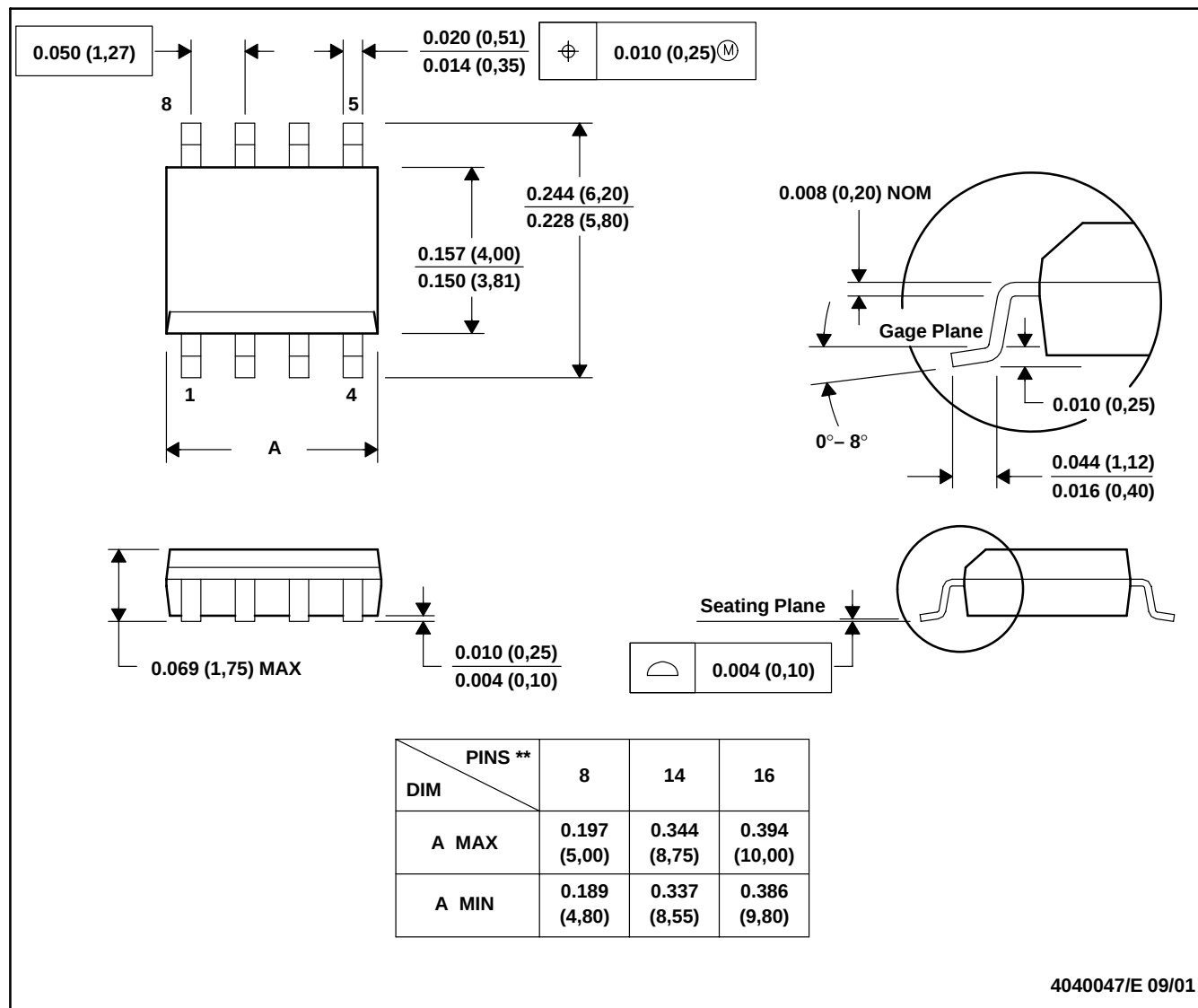
C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



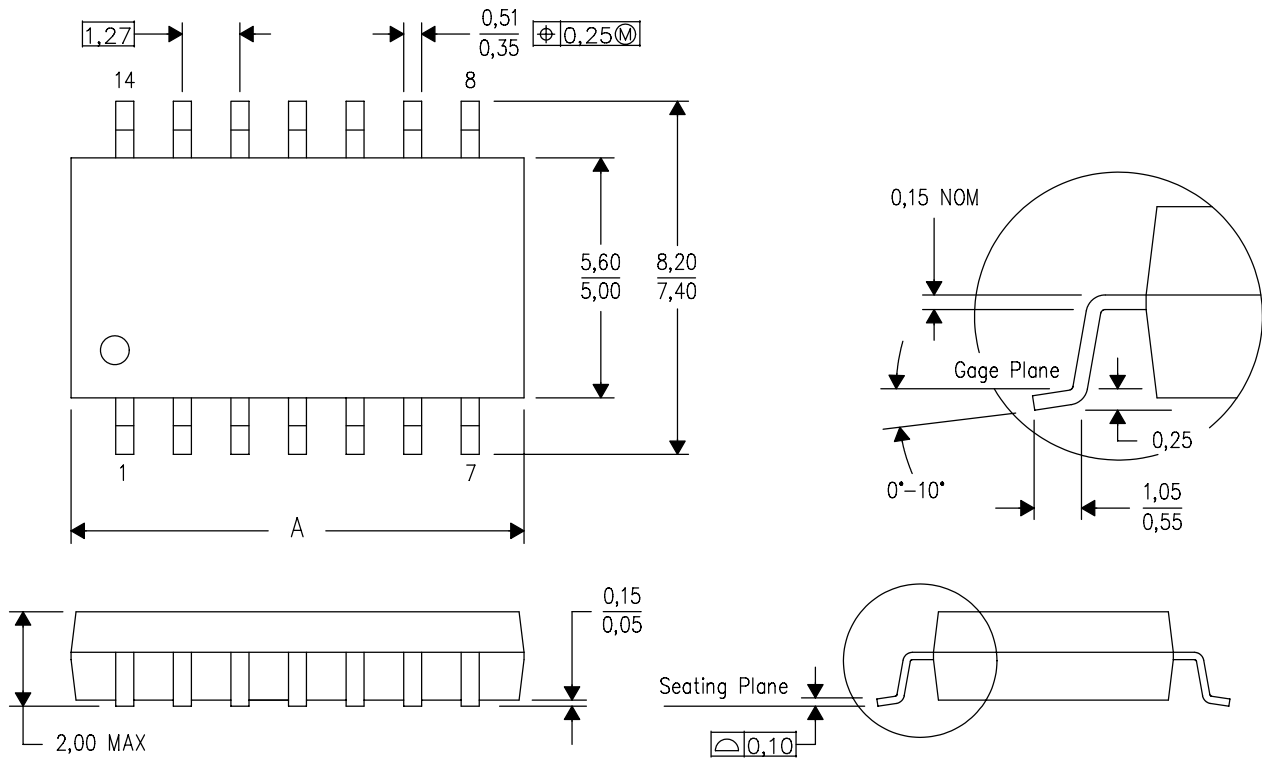
- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14    | 16    | 20    | 24    |
|---------------|-------|-------|-------|-------|
| A MAX         | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN         | 9,90  | 9,90  | 12,30 | 14,70 |

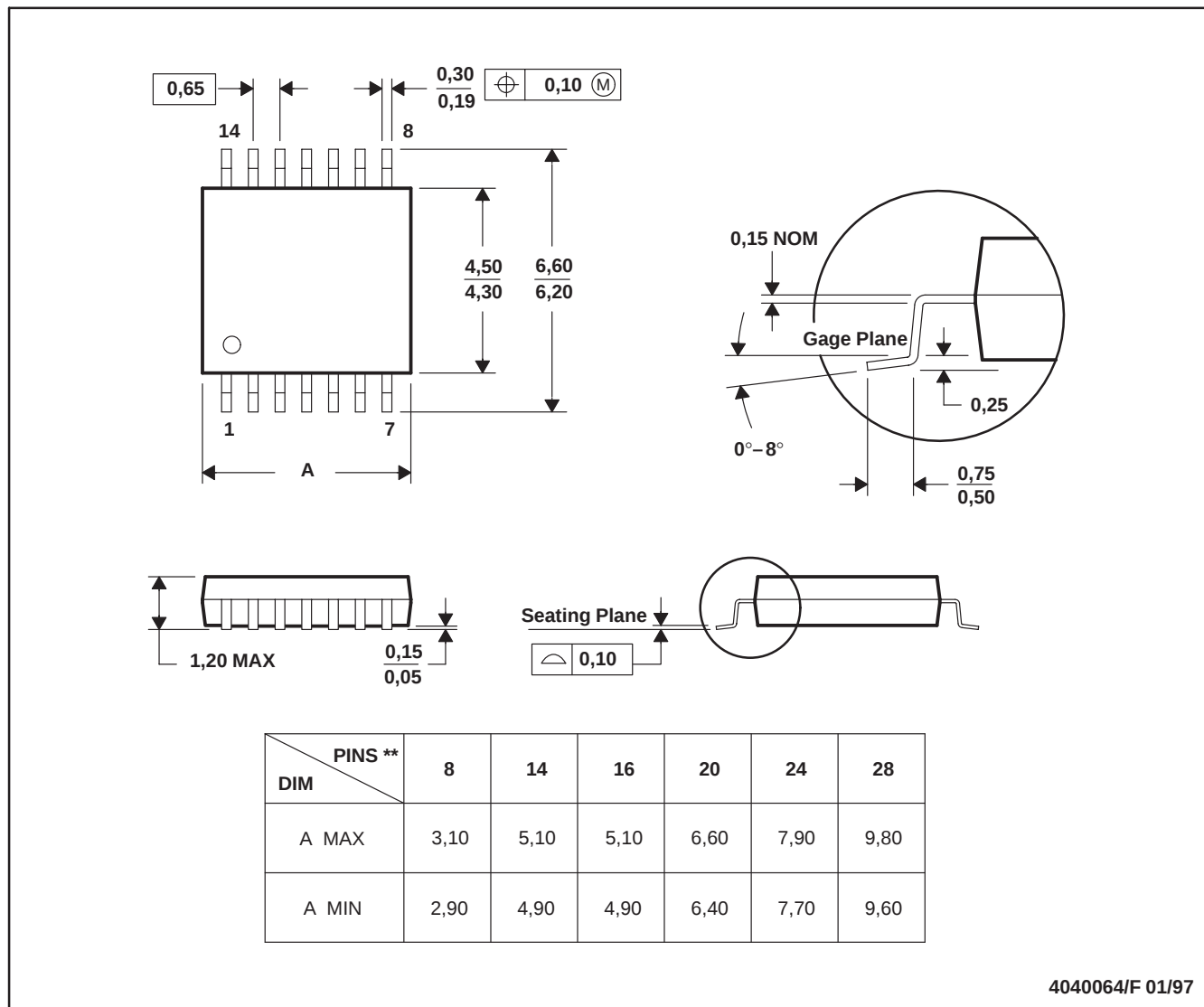
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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